FIG.1

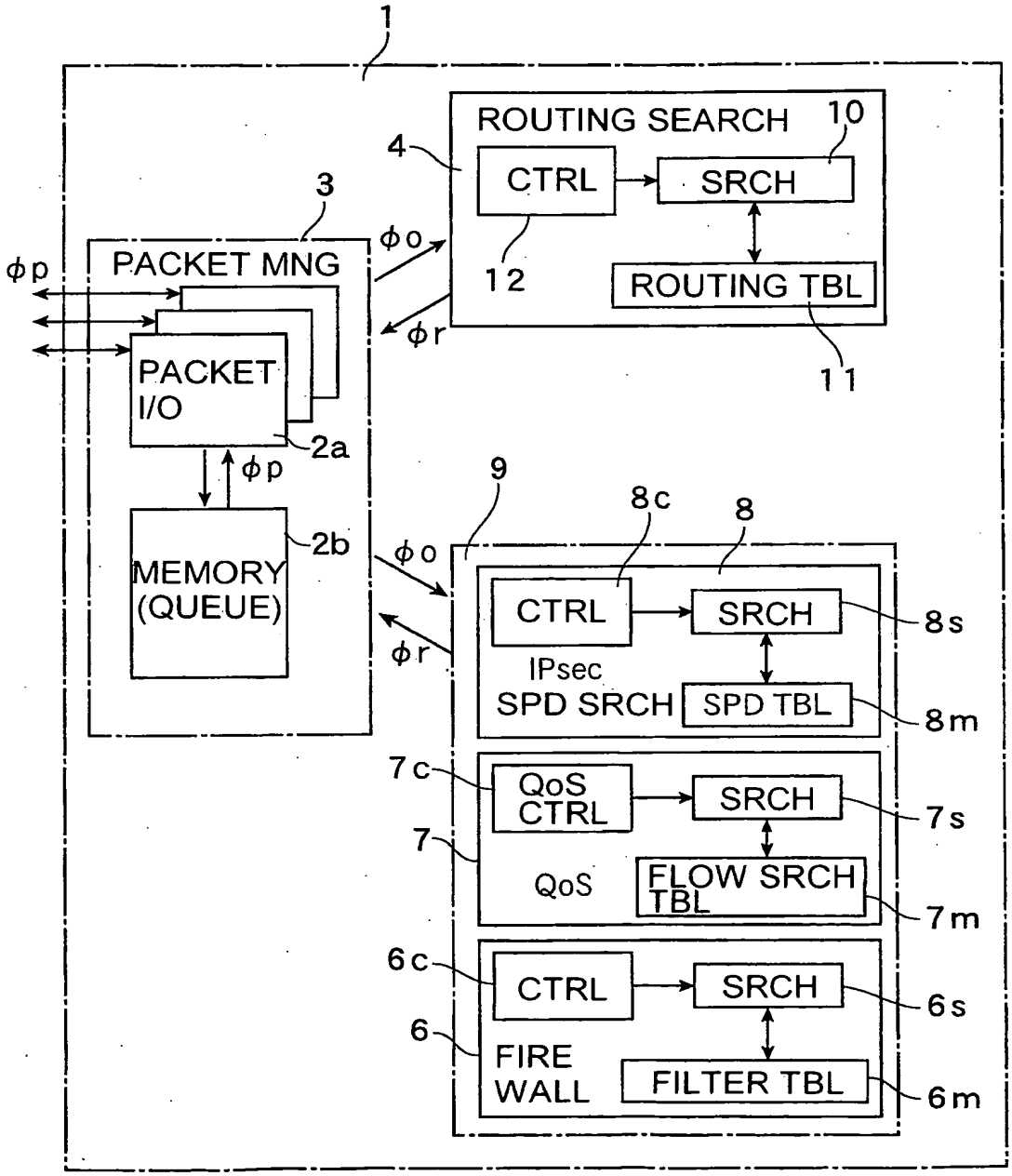

1
ROUTING SEARCH
10
4
CTRL
SRCH
3
φo
φp
PACKET MNG
12
ROUTING TBL
φr
11
PACKET I/O
2a
φp
9
8c
8
2b
φo
MEMORY (QUEUE)
CTRL
SRCH
8s
φr
IPsec SPD SRCH
SPD TBL
8m
7c
QoS CTRL
SRCH
7s
7
QoS
FLOW SRCH TBL
7m
6c
CTRL
SRCH
6s
6
FIRE WALL
FILTER TBL
6m

FIG.2

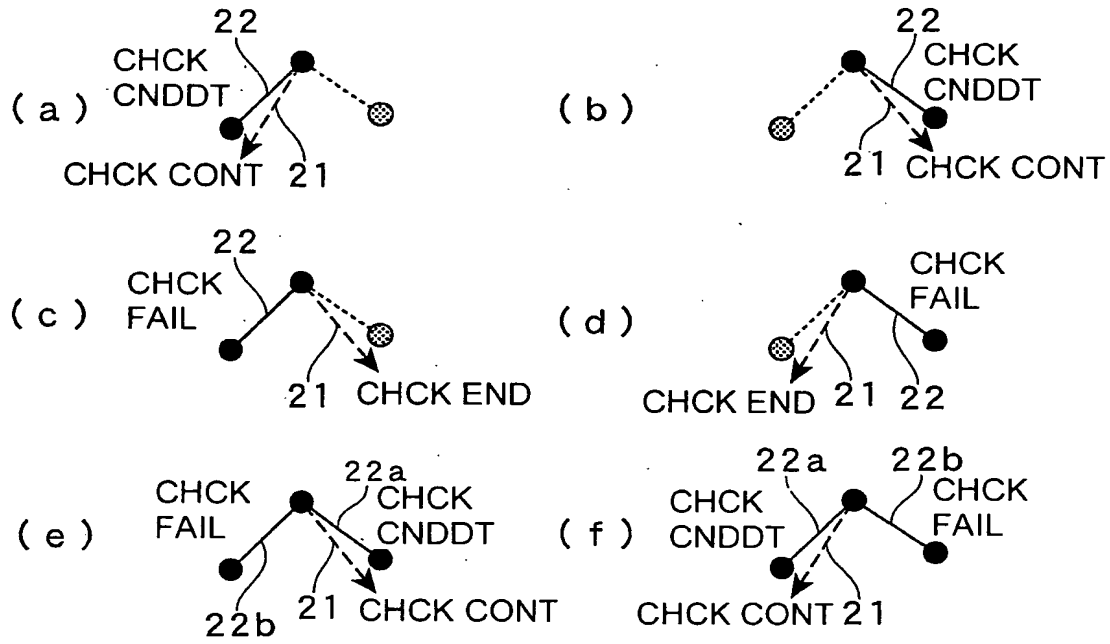

(a)
22
CHCK
CNDDT
CHCK CONT
21
(b)
22
CHCK
CNDDT
21
CHCK CONT
(c)
22
CHCK
FAIL
21
CHCK END
(d)
CHCK
FAIL
CHCK END
21
22
(e)
CHCK
FAIL
22a
CHCK
CNDDT
22b
21
CHCK CONT
(f)
22a
22b
CHCK
CNDDT
CHCK
FAIL
CHCK CONT
21

FIG.3

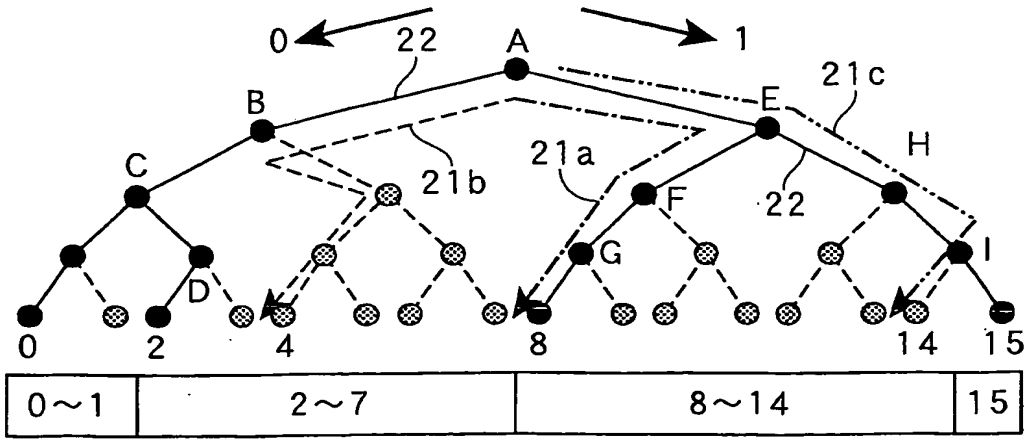

0
22
A
1
21c
B
E
H
C
21b
21a
F
22
G
I
D
0
2
4
8
14
15
0～1
2～7
8～14
15

FIG.4

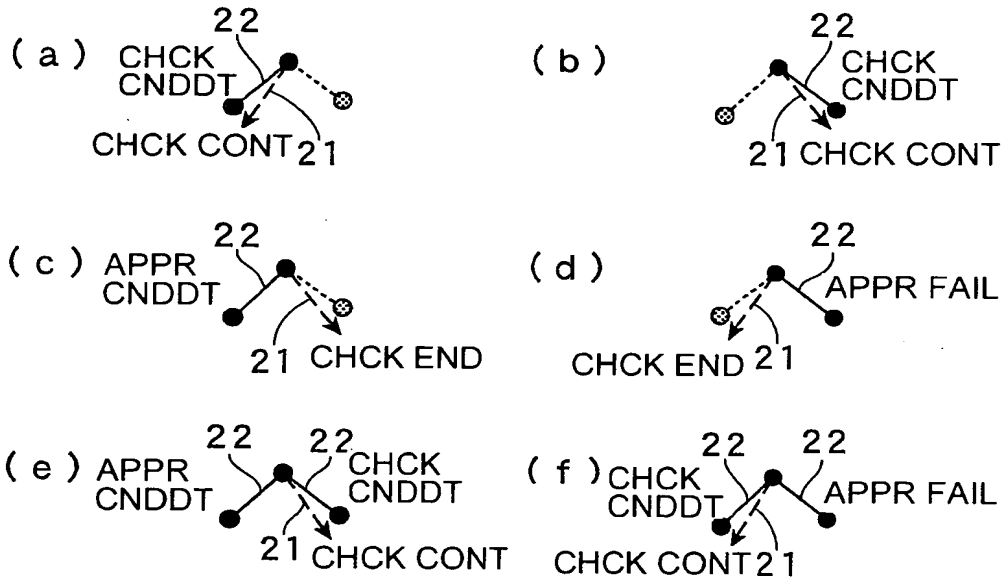

(a)
22
CHCK
CNDDT
CHCK CONT
21
(b)
22
CHCK
CNDDT
21
CHCK CONT
(c)
APPR
CNDDT
22
21
CHCK END
(d)
22
APPR FAIL
CHCK END
21
(e)
APPR
CNDDT
22
22
CHCK
CNDDT
21
CHCK CONT
(f)
CHCK
CNDDT
22
22
APPR FAIL
CHCK CONT
21

FIG.5

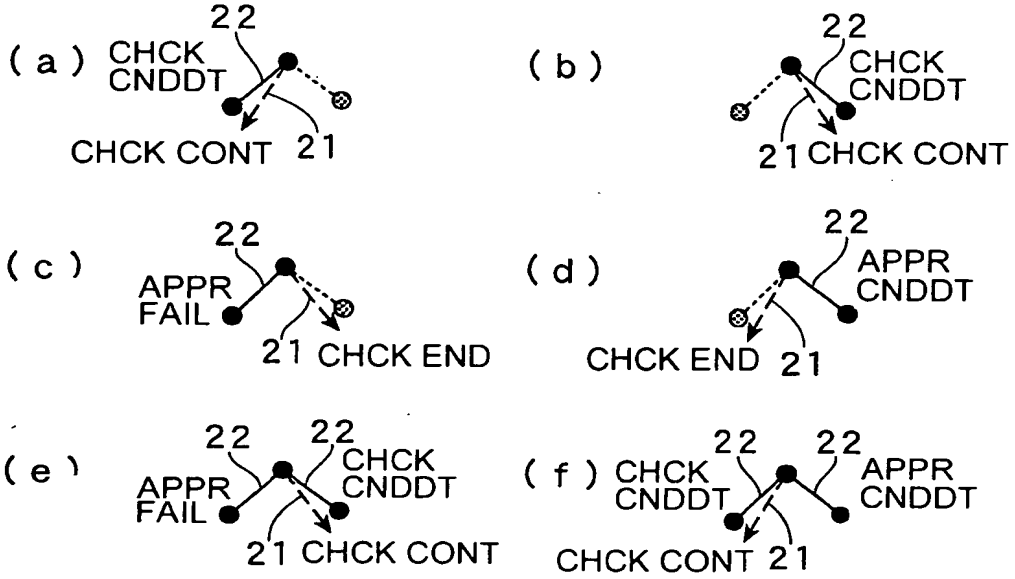

(a)
CHCK
CNDDT
22
CHCK CONT
21
(b)
22
CHCK
CNDDT
21
CHCK CONT
(c)
22
APPR
FAIL
21
CHCK END
(d)
22
APPR
CNDDT
CHCK END
21
(e)
22
22
APPR
FAIL
CHCK
CNDDT
21
CHCK CONT
(f)
CHCK
CNDDT
22
22
APPR
CNDDT
CHCK CONT
21

FIG.6

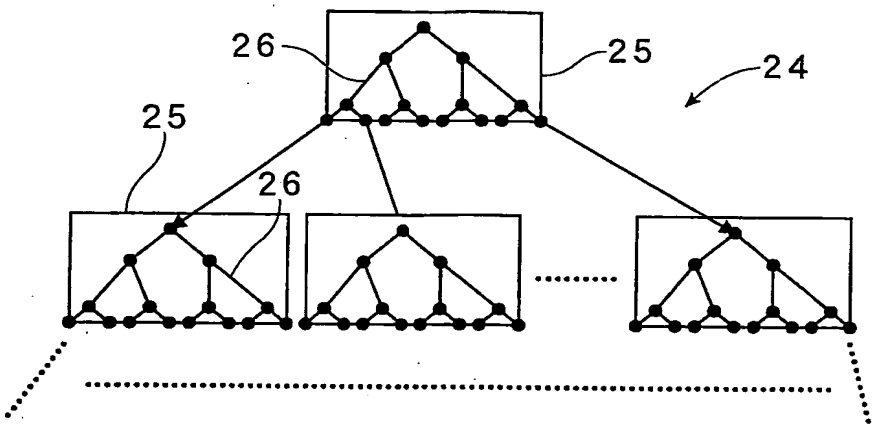

26
25
24
25
26

FIG.7

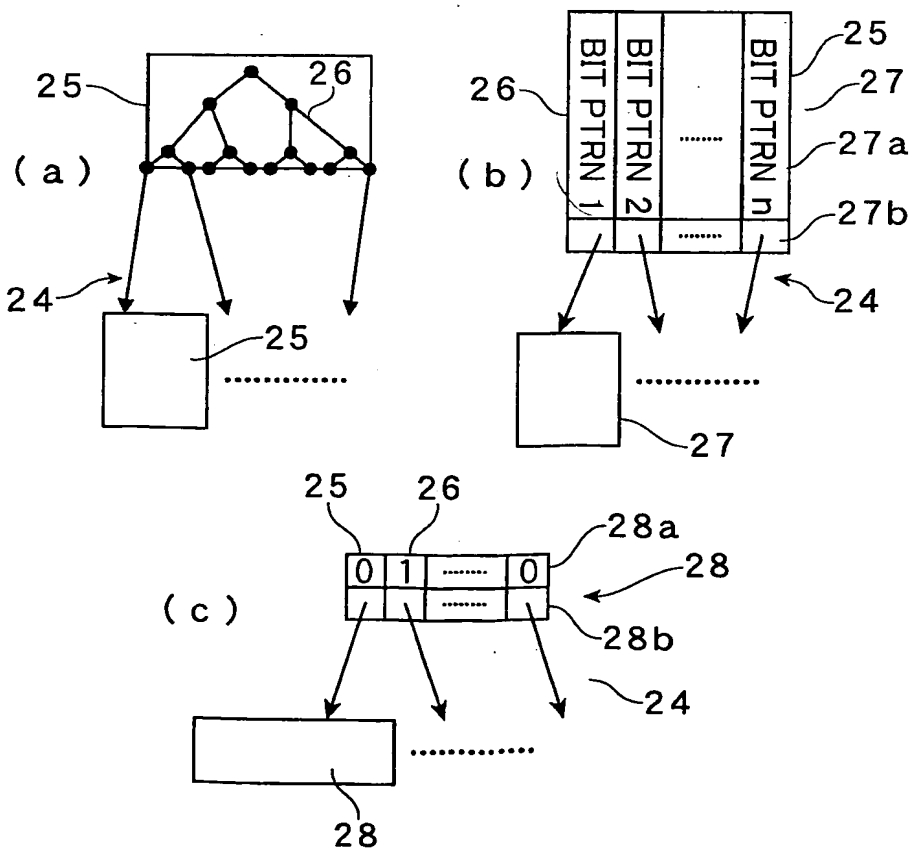
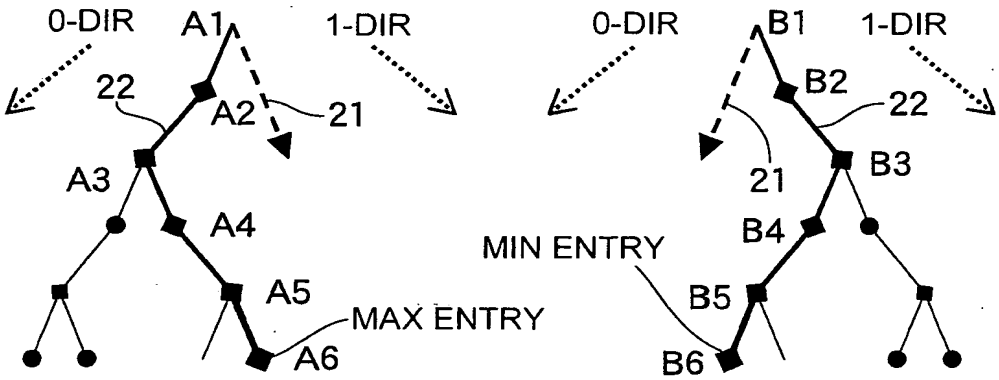
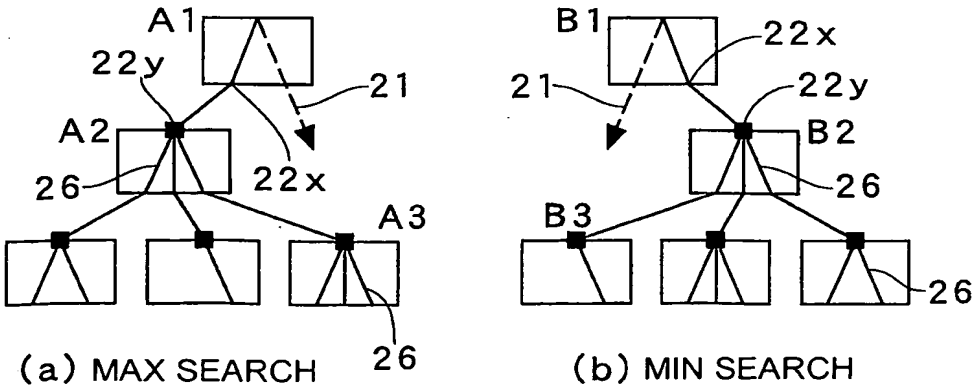

25
26
(a)
24
25
(b)
BIT PTRN 1
BIT PTRN 2
BIT PTRN n
25
27
27a
27b
26
24
27
(c)
25
26
28a
0
1
0
28
28b
24
28

FIG.8



(a) MAX SEARCH (b) MIN SEARCH

FIG.9



(a) MAX SEARCH (b) MIN SEARCH

FIG.10

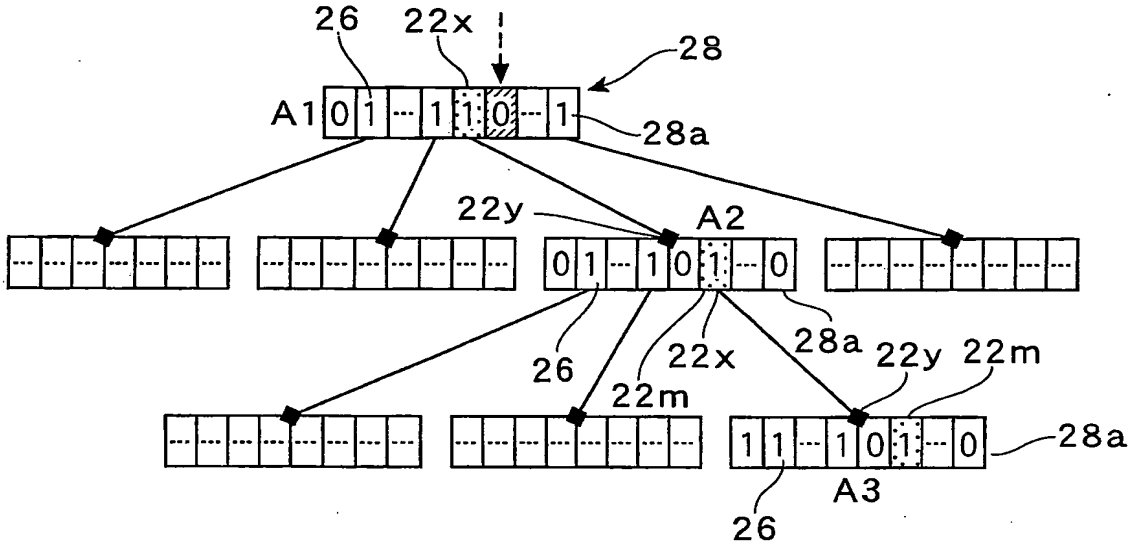
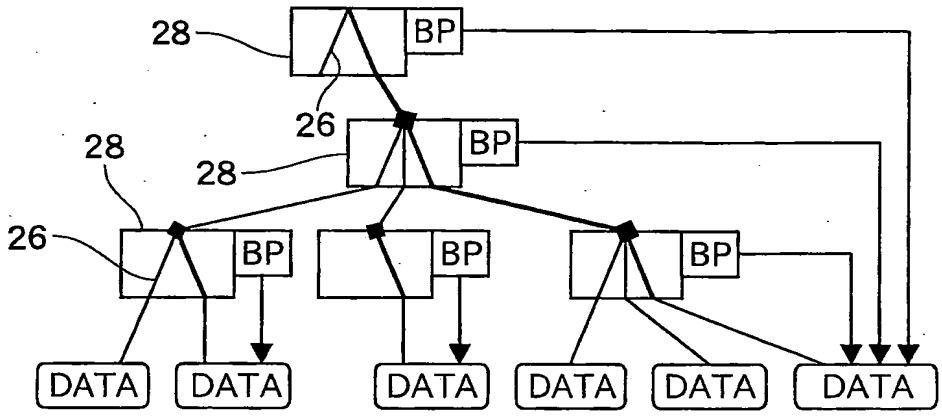
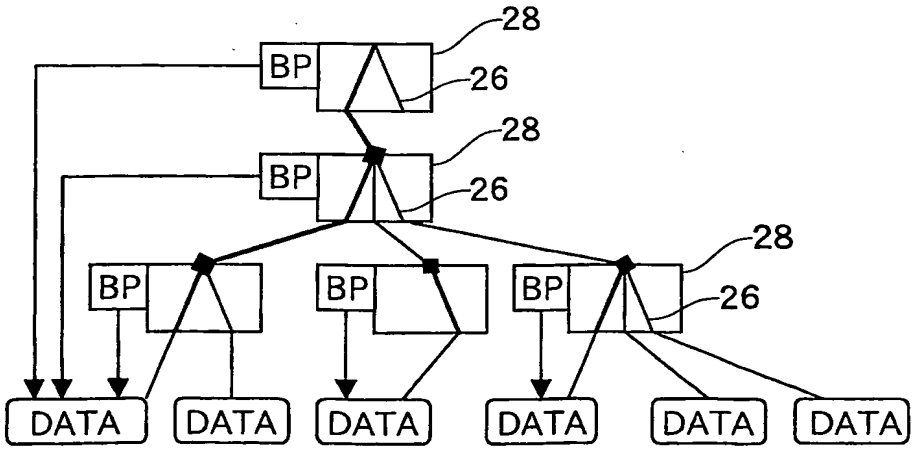

26
22x
28
A1
0 1 ··· 1 1 0 ··· 1
28a
22y
A2
0 1 ··· 1 0 1 ··· 0
26
22x
28a
22y
22m
22m
1 1 ··· 1 0 1 ··· 0
28a
A3
26

FIG.11



(a) MAX BYPAS



(b) MIN BYPASS

FIG.12

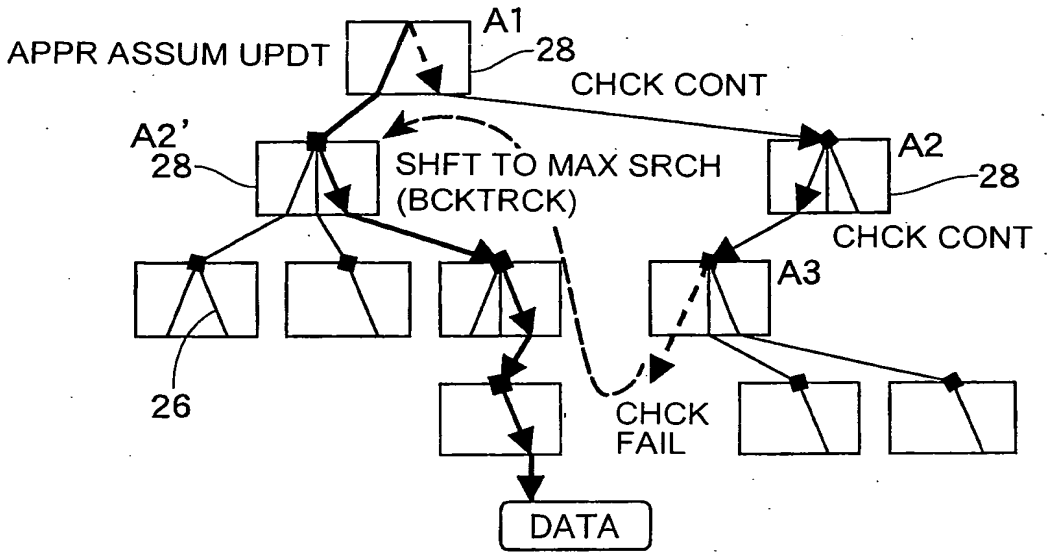
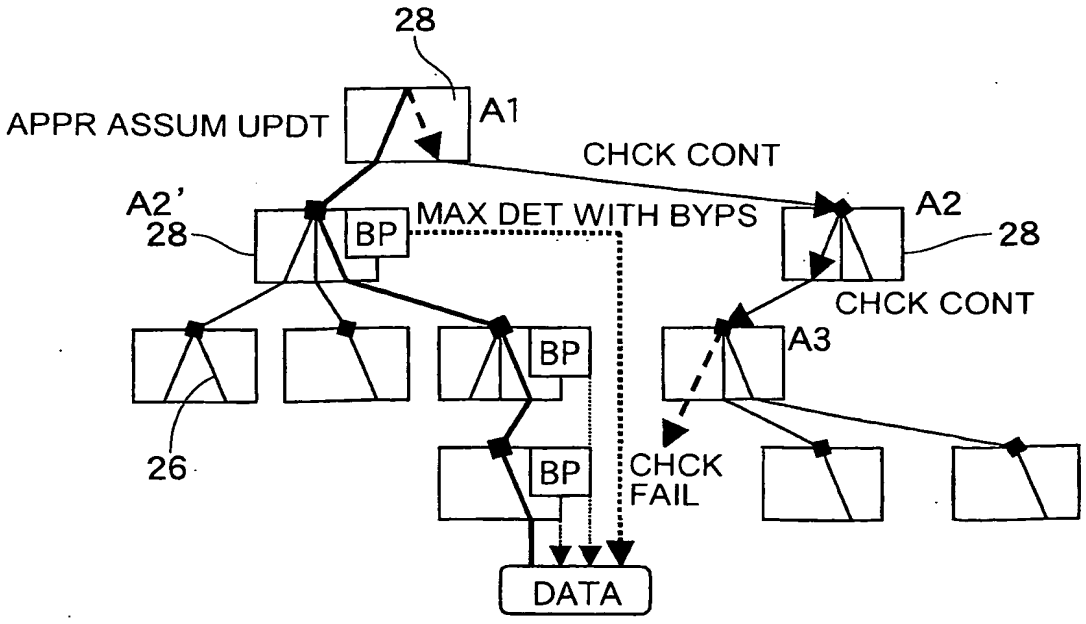

APPR ASSUM UPDT
A1
28
CHCK CONT
A2'
28
SHFT TO MAX SRCH
(BCKTRCK)
A2
28
CHCK CONT
A3
26
CHCK
FAIL
DATA

FIG.13


28
APPR ASSUM UPDT
A1
CHCK CONT
A2'
28
BP
MAX DET WITH BYPS
A2
28
CHCK CONT
A3
BP
BP
26
CHCK
FAIL
DATA

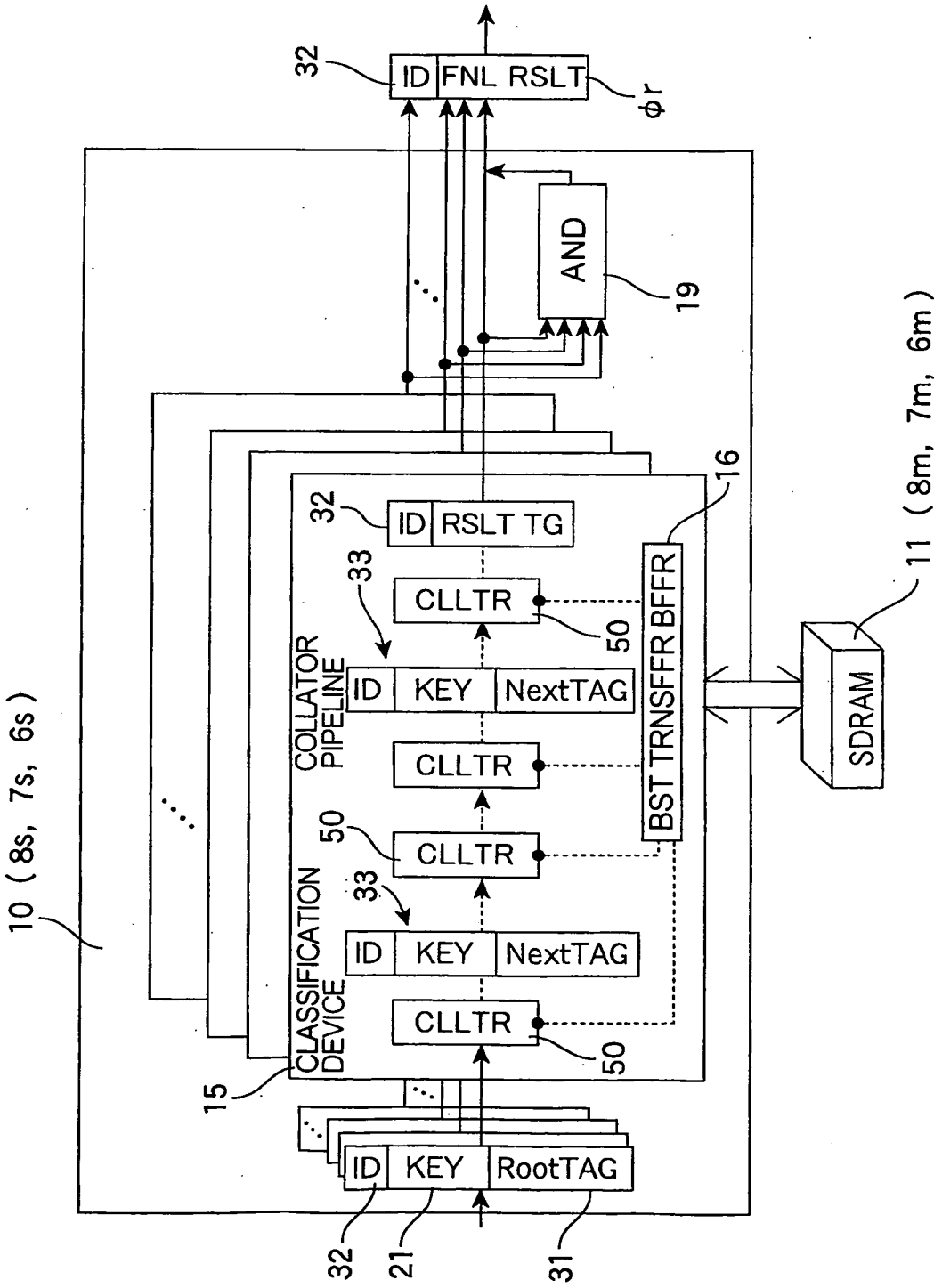

32
ID
FNL RSLT
φr
AND
19
16
32
ID
RSLT TG
33
CLLTR
50
BST TRNSFR BFFR
11 (8m, 7m, 6m)
SDRAM
COLLATOR PIPELINE
ID
KEY
NextTAG
CLLTR
50
33
ID
KEY
NextTAG
CLLTR
50
CLASSIFICATION DEVICE
10 (8s, 7s, 6s)
15
ID
KEY
RootTAG
32
21
31

FIG.14

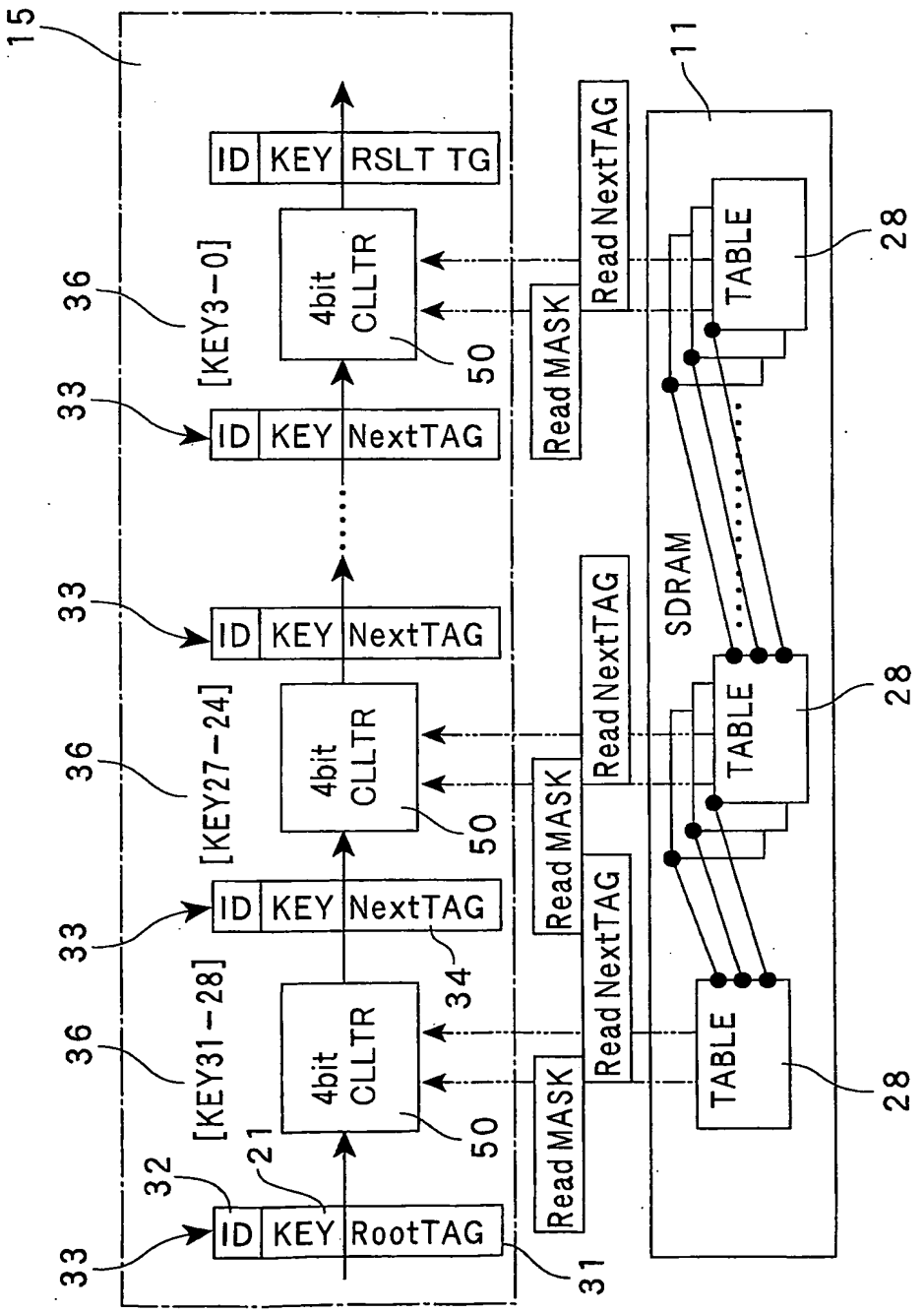
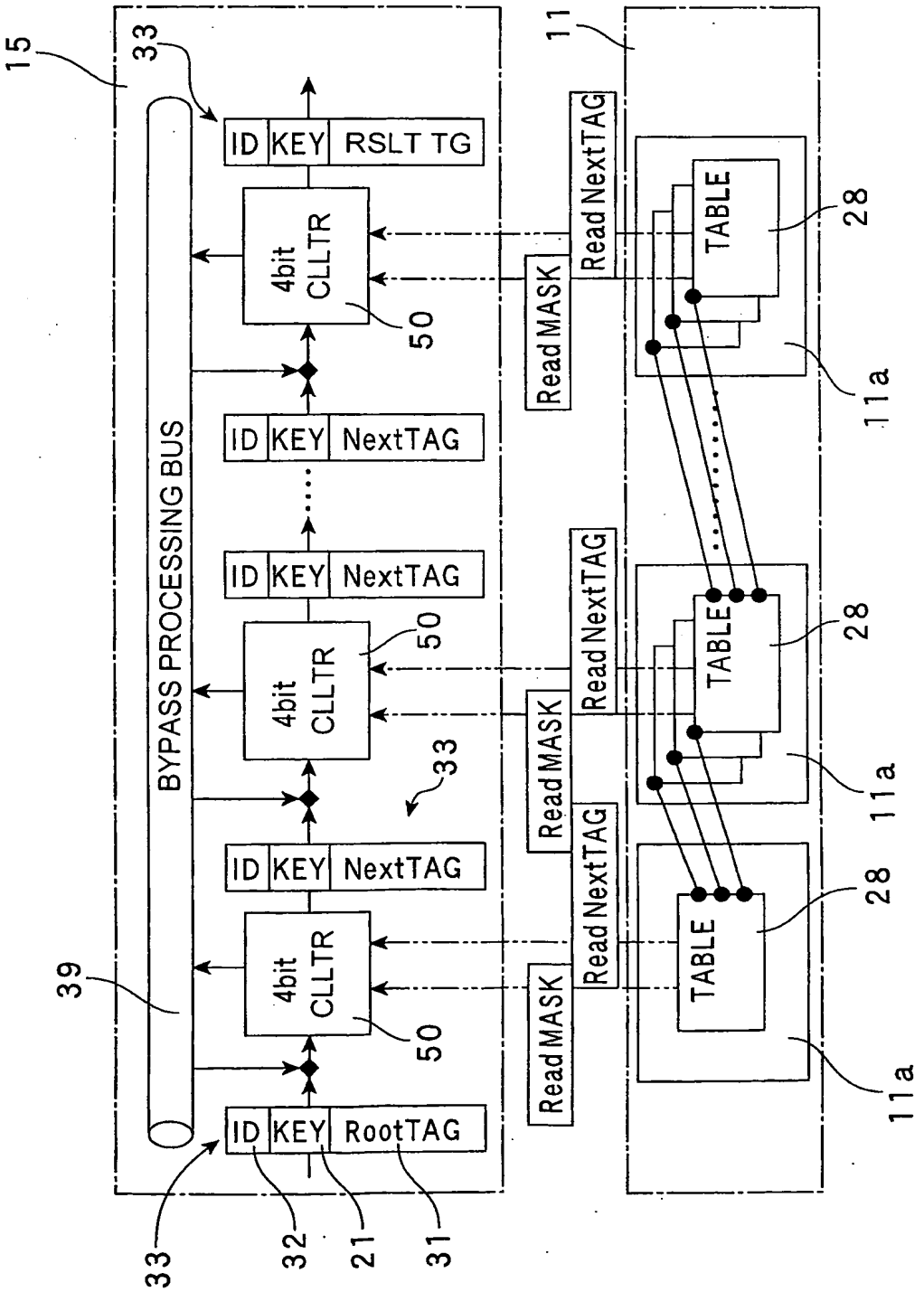

15
11
ID KEY RSLT TG
4bit CLLTR
[KEY3-0]
ID KEY NextTAG
4bit CLLTR
[KEY27-24]
ID KEY NextTAG
4bit CLLTR
[KEY31-28]
ID KEY RootTAG
Read MASK
Read NextTAG
SDRAM
TABLE
28
36
33
50
34
21
32
31

FIG.15

FIG.16


15
33
11
ID KEY RSLT TG
4bit CLLTR
50
ID KEY NextTAG
ID KEY NextTAG
4bit CLLTR
50
33
ID KEY NextTAG
4bit CLLTR
50
ID KEY RootTAG
BYPASS PROCESSING BUS
39
Read MASK
Read NextTAG
Read MASK
Read NextTAG
Read MASK
Read NextTAG
TABLE
28
11a
TABLE
28
11a
TABLE
28
11a
33
32
21
31

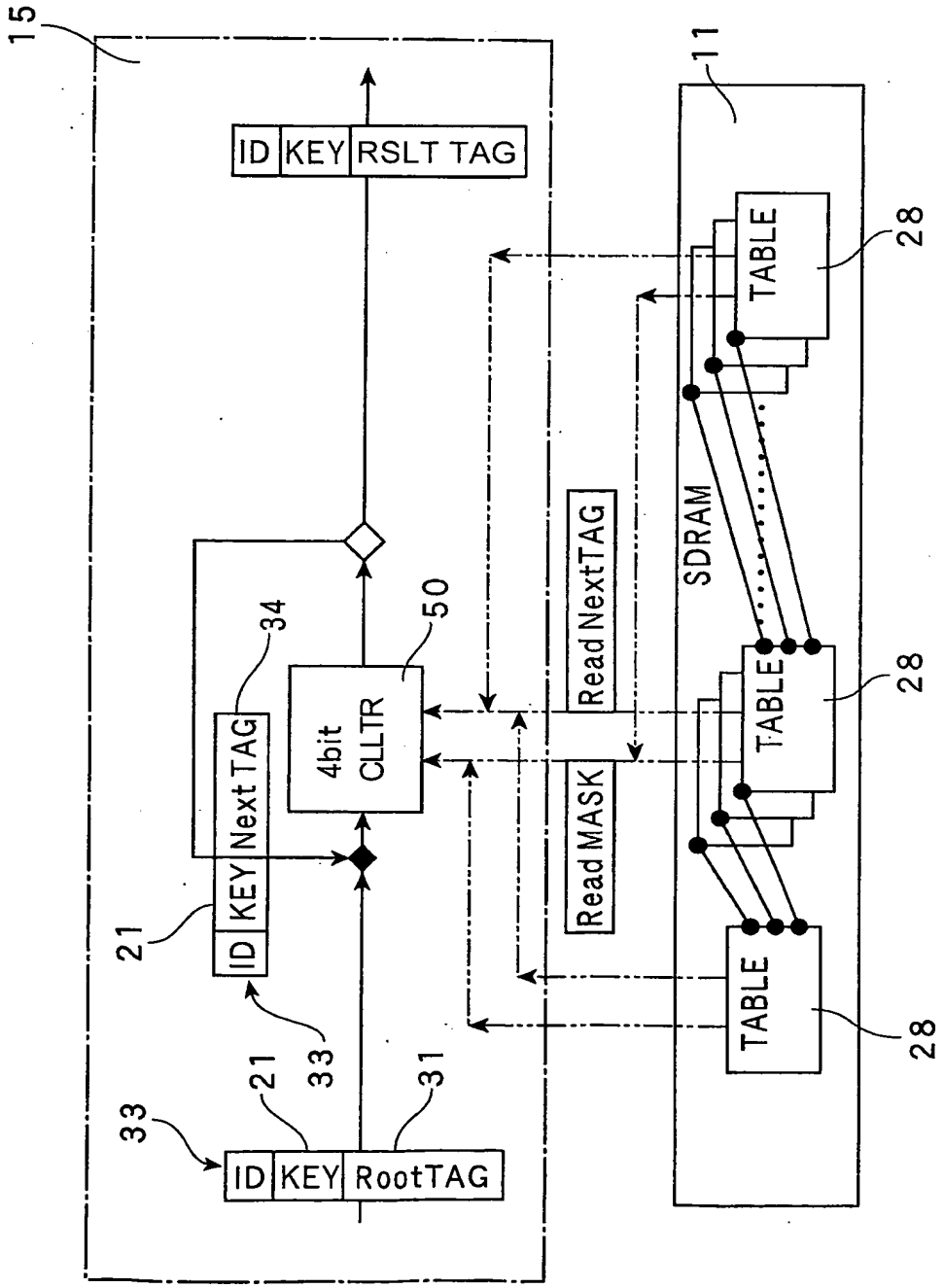

15
11
ID KEY RSLT TAG
TABLE
28
SDRAM
Read NextTAG
Read MASK
4bit CLLTR
50
34
ID KEY Next TAG
21
33
31
ID KEY RootTAG

FIG.17

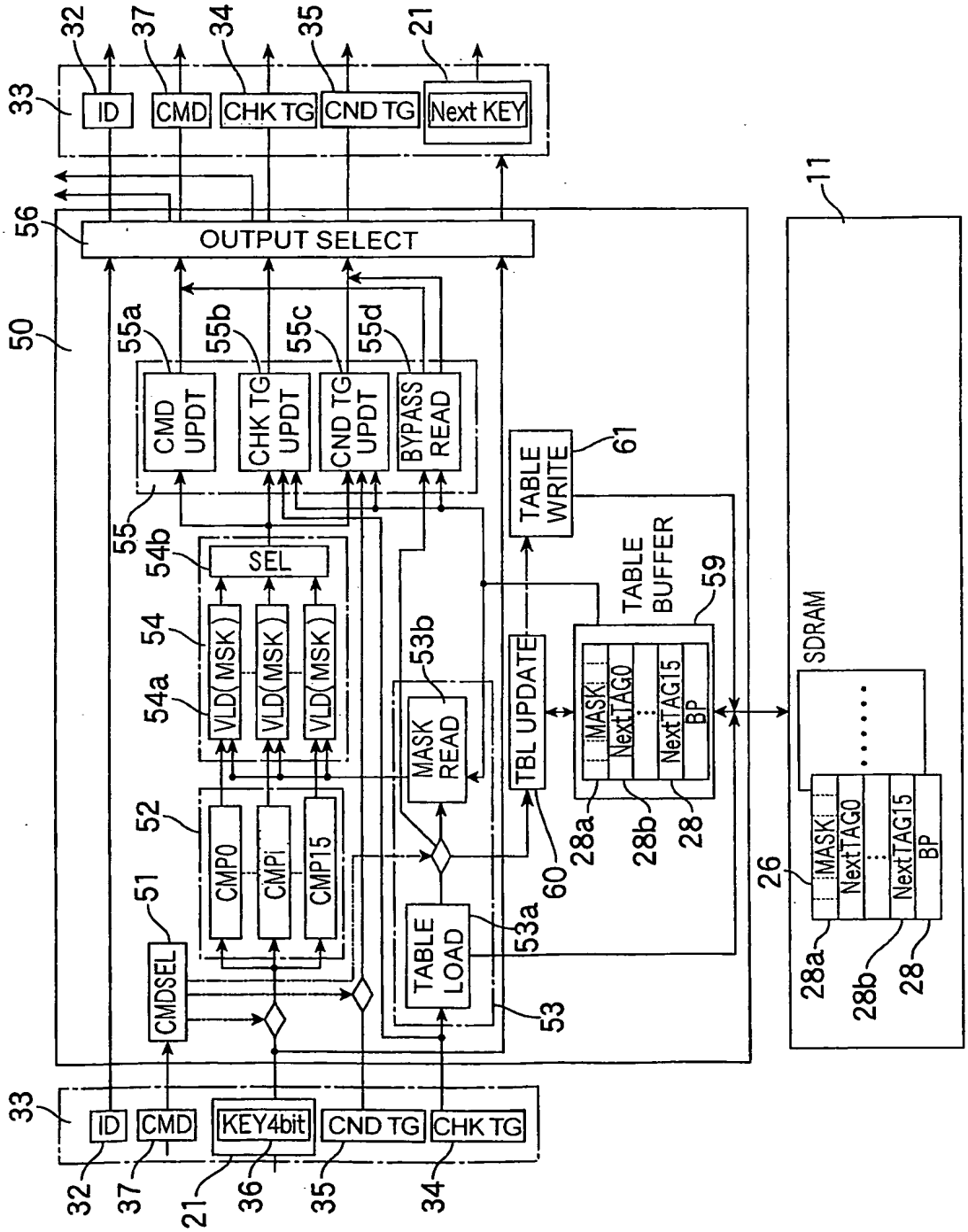
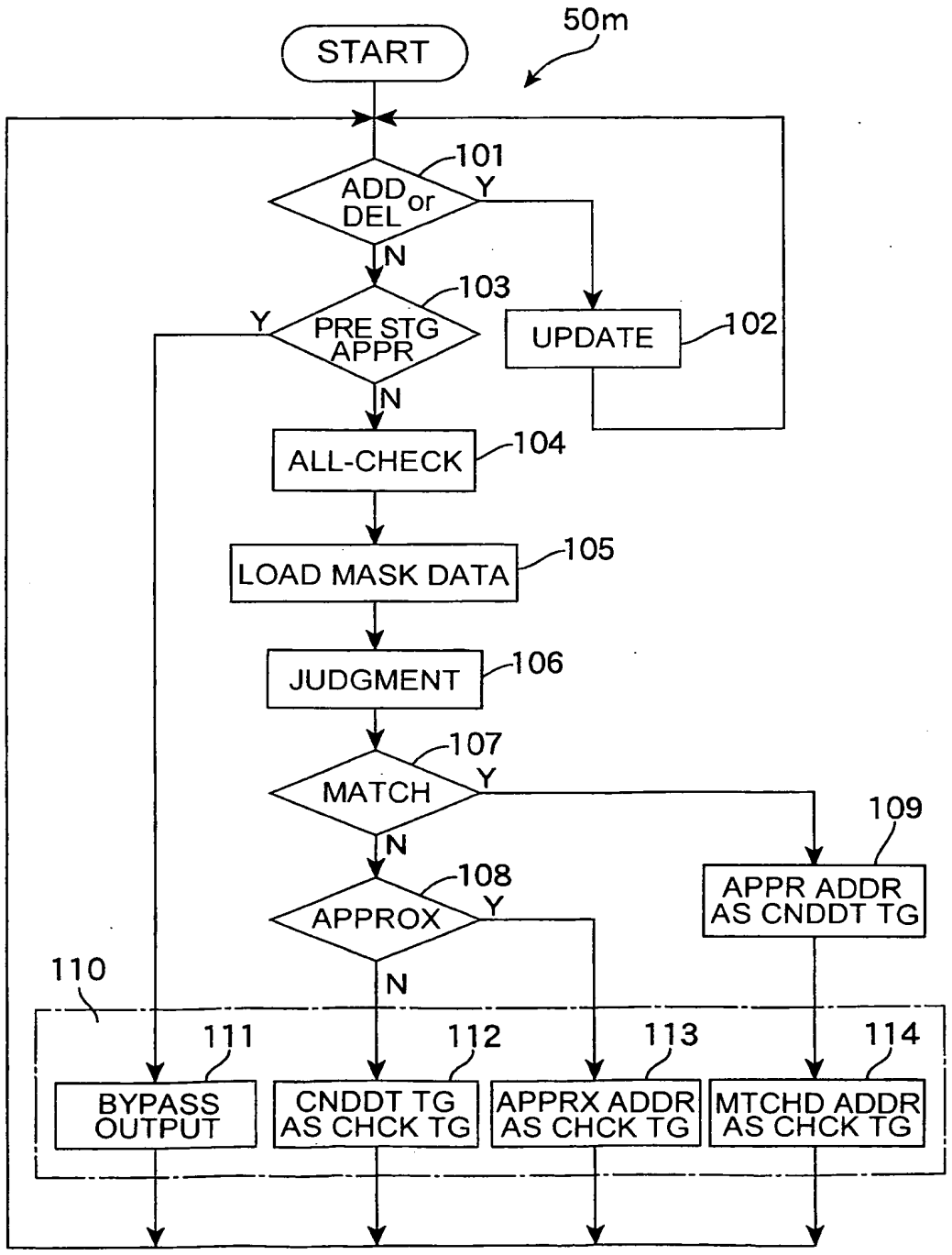

ID
CMD
CHK TG
CND TG
Next KEY
OUTPUT SELECT
CMD UPDT
CHK TG UPDT
CND TG UPDT
BYPASS READ
SEL
VLD(MSK)
CMP0
CMPi
CMP15
CMDSEL
MASK READ
TABLE LOAD
TBL UPDATE
TABLE WRITE
TABLE BUFFER
iMASK
NextTAG0
NextTAG15
BP
SDRAM
KEY4bit
32
37
34
35
21
33
56
50
55a
55b
55c
55d
55
54b
54
54a
53b
52
51
53a
53
60
61
59
28a
28b
28
26
36
11

FIG.18

FIG.19


50m
START
101
ADD or DEL
Y
N
103
PRE STG APPR
Y
N
UPDATE
102
ALL-CHECK
104
LOAD MASK DATA
105
JUDGMENT
106
107
MATCH
Y
N
109
APPR ADDR AS CNDDT TG
108
APPROX
Y
N
110
111
112
113
114
BYPASS OUTPUT
CNDDT TG AS CHCK TG
APPRX ADDR AS CHCK TG
MTCHD ADDR AS CHCK TG

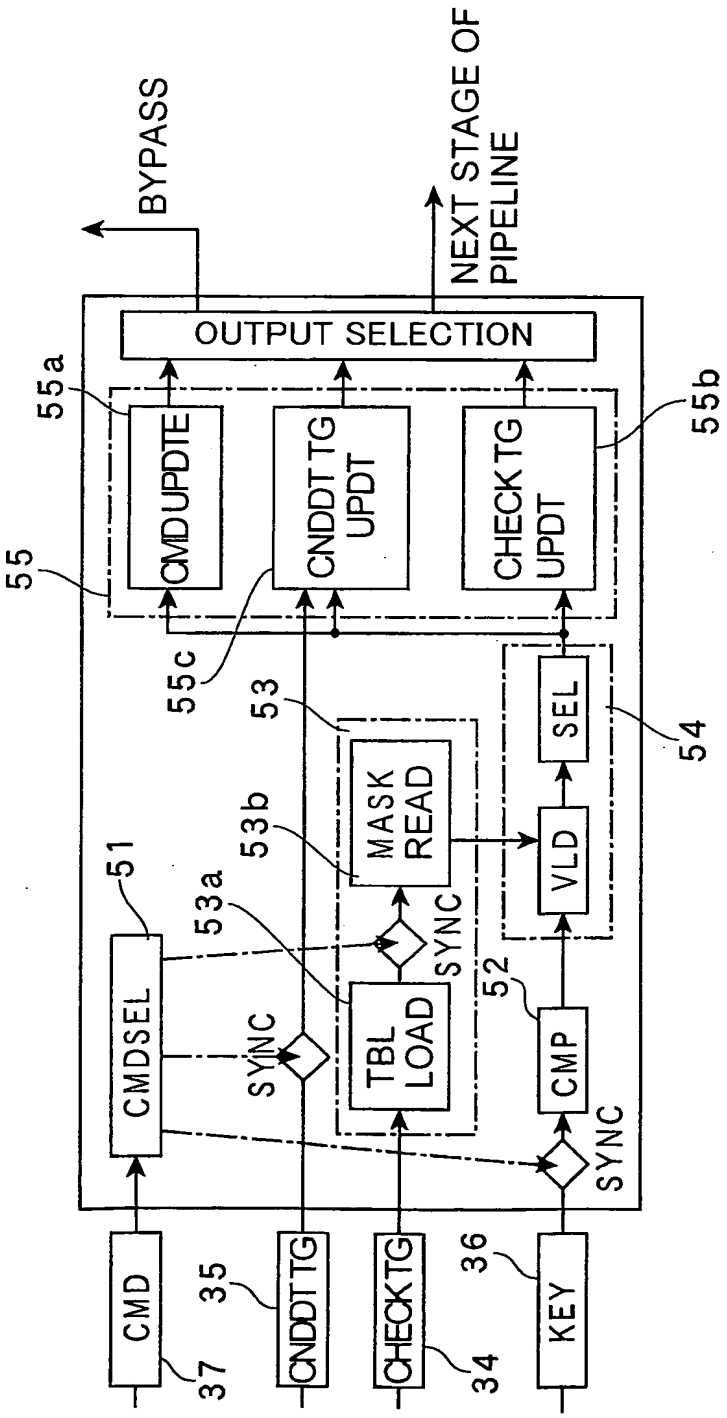

BYPASS
NEXT STAGE OF PIPELINE
OUTPUT SELECTION
55a
55b
55
55c
CMDUPDTE
CNDDT TG UPDT
CHECK TG UPDT
53
53b
MASK READ
SEL
54
VLD
51
53a
SYNC
CMDSEL
TBL LOAD
52
CMP
SYNC
SYNC
CMD
35
CNDDT TG
CHECK TG
36
KEY
37
34

FIG.20

FIG.21

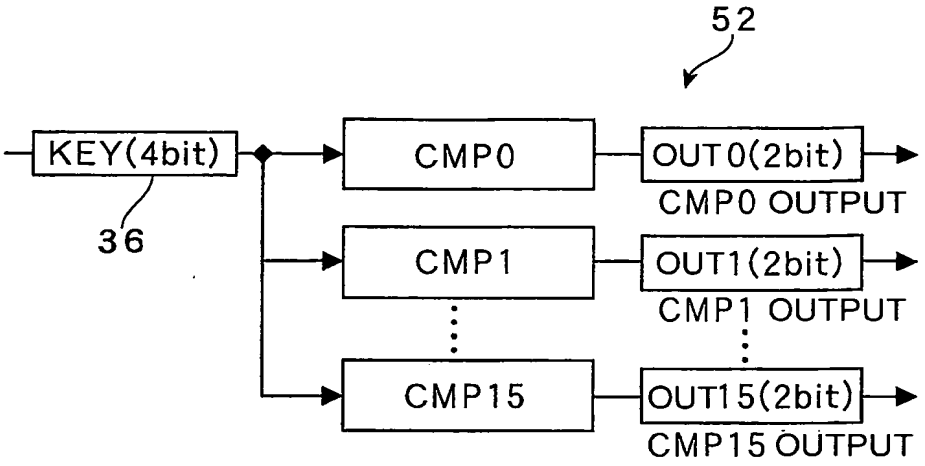


FIG.22

LOGIC OF COMPARATOR CMPi

CMPi INPUT x	OUTPUT
x＜i	10 (「＜」)
x＝i	01 (「＝」)
x＞i	11 (「＞」)
i＝0～15 (FIXED VALUE) x＝0～15 (4 bit INPUT VALUE)	

FIG.23

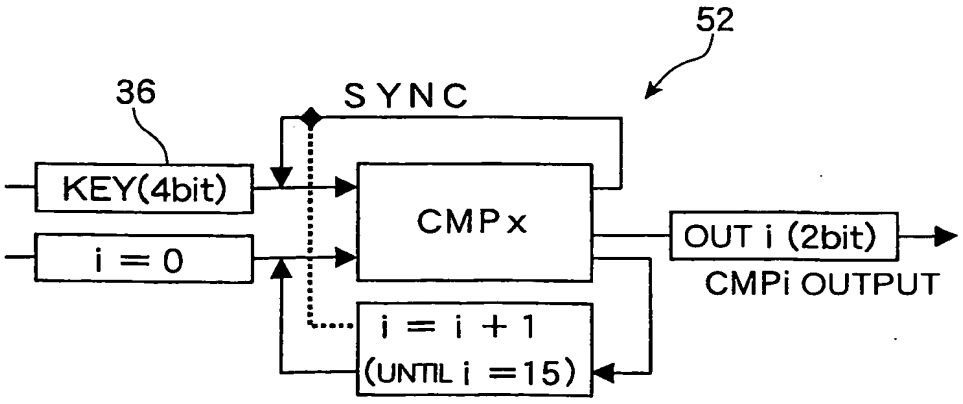


FIG.24

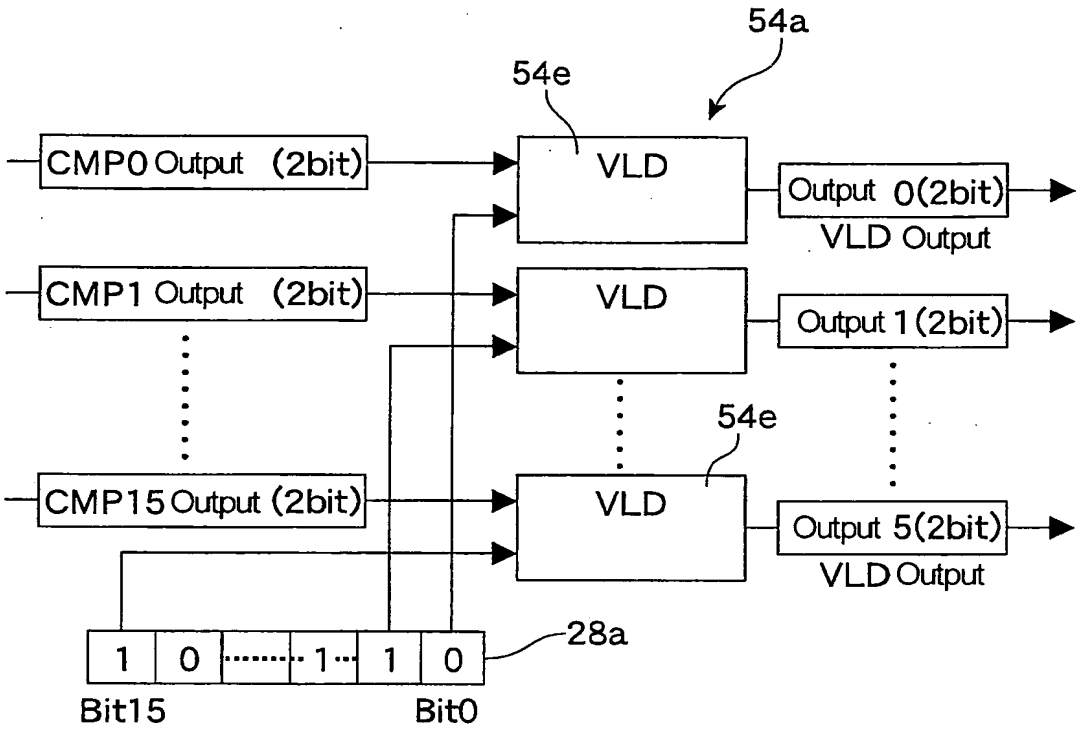


FIG.25

LOGIC OF MASK DEVICE VLD

CMPi Output	MASK VAL	VLD Output
10	0	00 (「X」)
01	0	00 (「X」)
11	0	00 (「X」)
10	1	10 (「<」)
01	1	01 (「=」)
11	1	11 (「>」)
AND OPERATION WITH MASK VAL		

FIG.26

SELECTION LOGIC OF COMPLETE MATCH SEARCH

V L D Output	Output Gf
00 (「×」)	0
10 (「<」)	0
01 (「=」)	1
11 (「>」)	0

FIG.27

SELECTION LOGIC OF SCOPE SEARCH
(RIGHT-INCLINED MATCH TYPE)

(a)

V L D Output	Intermediate Fr	Output Gr
00 (「×」)	0	0
10 (「<」)	0	0
01 (「=」)	0	0
11 (「>」)	1	Gr (i)

(b)

Hr(i−1)	Fr(i)	Hr(i)
0	0	0
0	1	1
1	0	1
1	1	1

(c)

Hr(i−1)	Hr(i)	Gr(i)
0	0	0
0	1	1
1	0	0
1	1	0

FIG.28

SELECTION LOGIC OF SCOPE SEARCH
(LEFT-INCLINED MATCH TYPE)

(a)

V L D Output	Intermediate F_I	Output G_I
00 (「×」)	0	0
10 (「<」)	1	G_I (i)
01 (「=」)	0	0
11 (「>」)	0	0

(b)

H_I (i+1)	F_I (i)	H_I (i)
0	0	0
0	1	1
1	0	1
1	1	1

(c)

H_I (i+1)	H_I (i)	G_I (i)
0	0	0
0	1	1
1	0	0
1	1	0

FIG.29

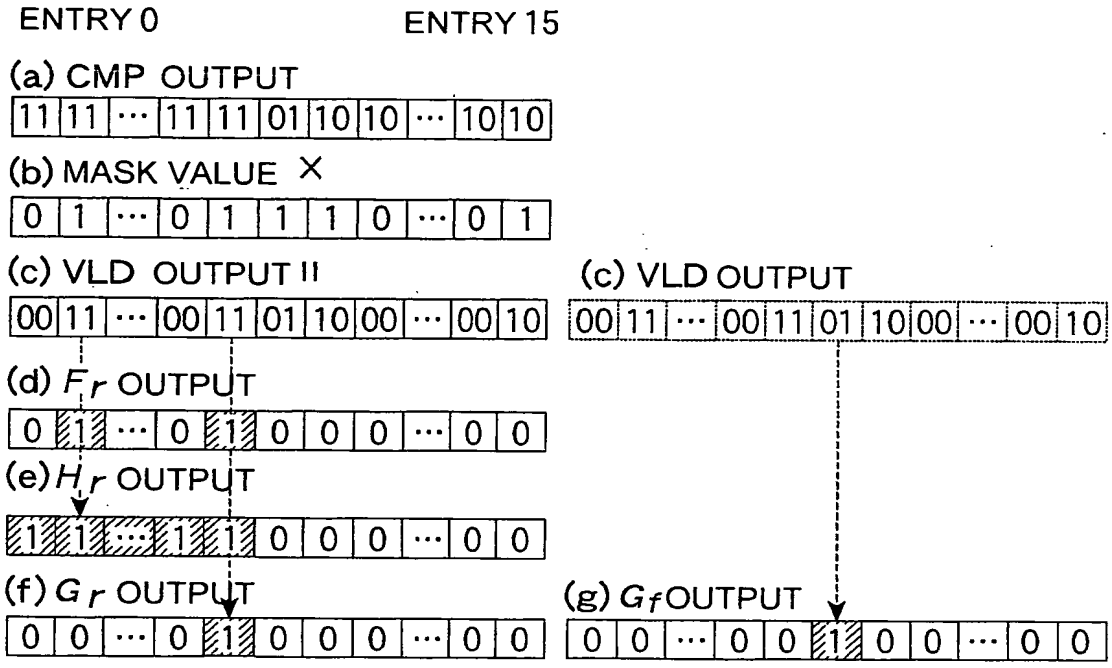

ENTRY 0
ENTRY 15
(a) CMP OUTPUT
11 11 ··· 11 11 01 10 10 ··· 10 10
(b) MASK VALUE ×
0 1 ··· 0 1 1 1 0 ··· 0 1
(c) VLD OUTPUT II
00 11 ··· 00 11 01 10 00 ··· 00 10
(c) VLD OUTPUT
00 11 ··· 00 11 01 10 00 ··· 00 10
(d) Fr OUTPUT
0 1 ··· 0 1 0 0 0 ··· 0 0
(e) Hr OUTPUT
1 1 ··· 1 1 0 0 0 ··· 0 0
(f) Gr OUTPUT
0 0 ··· 0 1 0 0 0 ··· 0 0
(g) Gf OUTPUT
0 0 ··· 0 0 1 0 0 ··· 0 0

FIG.30

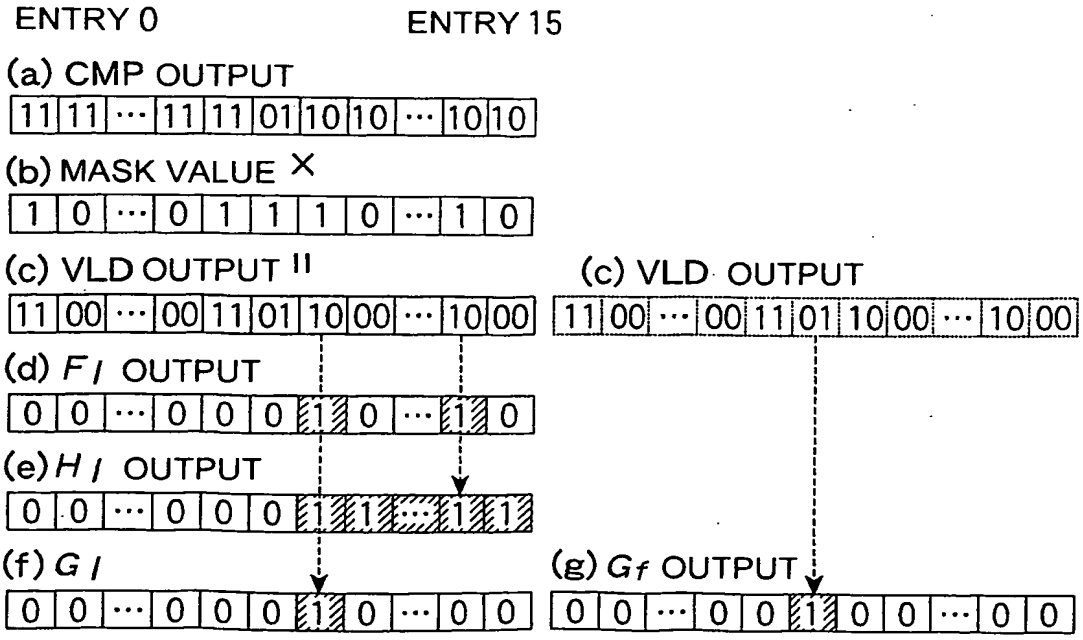

ENTRY 0
ENTRY 15
(a) CMP OUTPUT
11 11 ··· 11 11 01 10 10 ··· 10 10
(b) MASK VALUE ×
1 0 ··· 0 1 1 1 0 ··· 1 0
(c) VLD OUTPUT II
11 00 ··· 00 11 01 10 00 ··· 10 00
(c) VLD OUTPUT
11 00 ··· 00 11 01 10 00 ··· 10 00
(d) Fl OUTPUT
0 0 ··· 0 0 0 1 0 ··· 1 0
(e) Hl OUTPUT
0 0 ··· 0 0 0 1 1 ··· 1 1
(f) Gl
0 0 ··· 0 0 0 1 0 ··· 0 0
(g) Gf OUTPUT
0 0 ··· 0 0 1 0 0 ··· 0 0

FIG.31

37

TYPE	COMMAND	DESCRIPTION
COMPLETE MATCH SEARCH	FMATCHEXEC	CHECK CONT
	FMATCHHIT	HIT
	FMATCHFAIL	MISHIT
SCOPE SEARCH	MATCHEXEC	CHECK CONT
	MATCHRDBP	BYPASS READ
	MATCHFHIT	CMPLT MATCH HIT
	MATCHNHIT	APPROX HIT
	MATCHFAIL	MISHIT
REGISTRATION	ADD	HI → LO
	ADDNEW	NEW TABLE
	ADDFIN	REG CMPLT
	ADDFAIL	REG FAILURE
	ADDUPDT	BP UPDT FEED
	(ADDWCLR)	(WAIT CLEAR)
DELETION	DEL	LO CONTINUATIN
	DELFIN	DEL CMPLT
	DELFAIL	DEL FAILURE
	DELUPDT	BP UPDT FEED
	DELRDBP	LO BP REF
	DELWRBP	SELF BP UPDATE

FIG.32

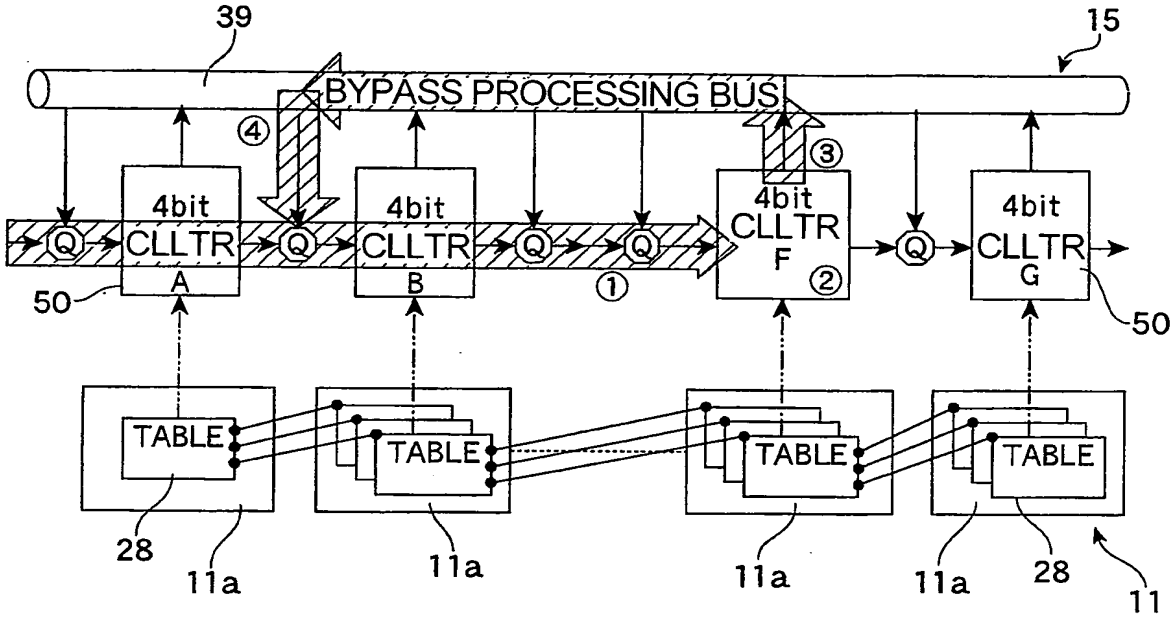

39
15
BYPASS PROCESSING BUS
④
③
4bit CLLTR A
4bit CLLTR B
4bit CLLTR F
4bit CLLTR G
Q
①
②
50
50
TABLE
28
11a
11a
11a
11a
28
11

FIG.33

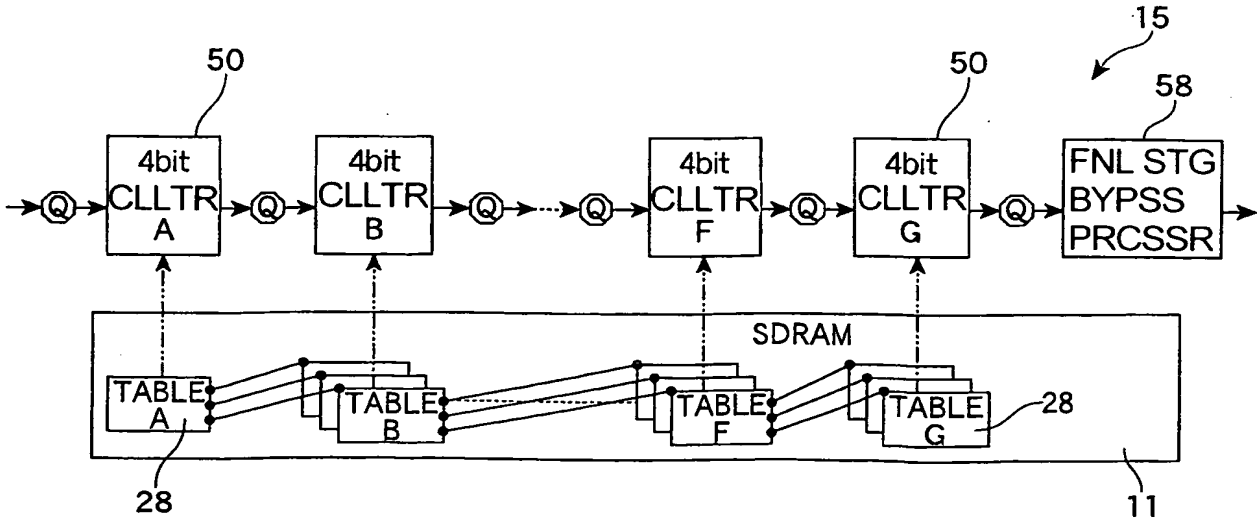

15
50
50
58
4bit CLLTR A
4bit CLLTR B
4bit CLLTR F
4bit CLLTR G
FNL STG BYPSS PRCSSR
Q
SDRAM
TABLE A
TABLE B
TABLE F
TABLE G
28
28
11

FIG.34

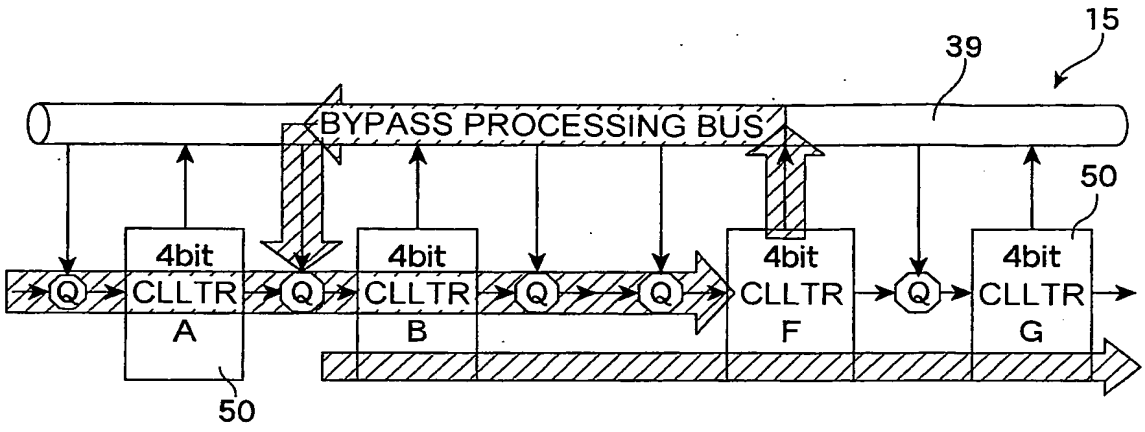

15
39
BYPASS PROCESSING BUS
50
4bit
CLLTR
A
4bit
CLLTR
B
4bit
CLLTR
F
4bit
CLLTR
G
Q
50

FIG.35

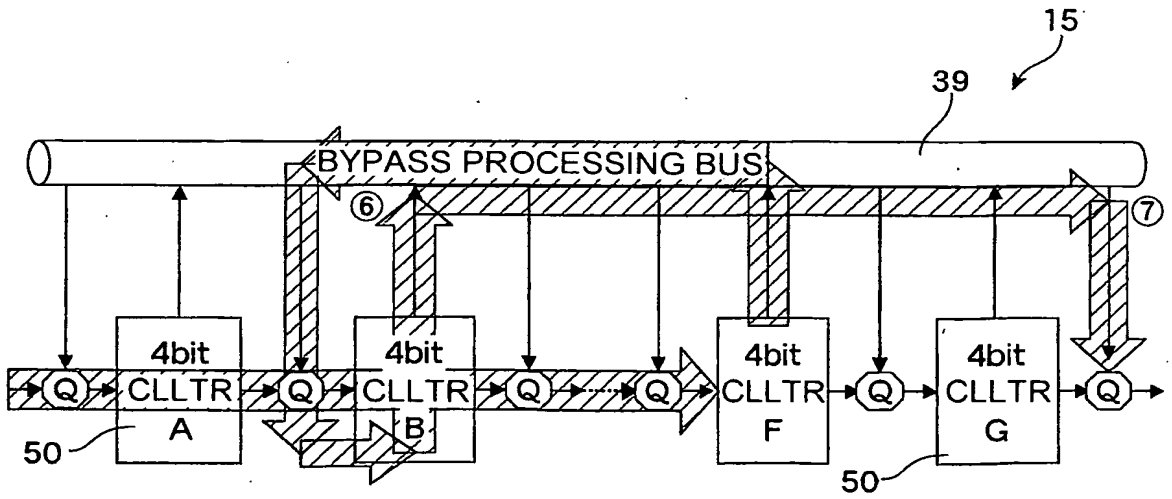

15
39
BYPASS PROCESSING BUS
⑥
⑦
4bit
CLLTR
A
4bit
CLLTR
B
4bit
CLLTR
F
4bit
CLLTR
G
Q
50
50

FIG.36

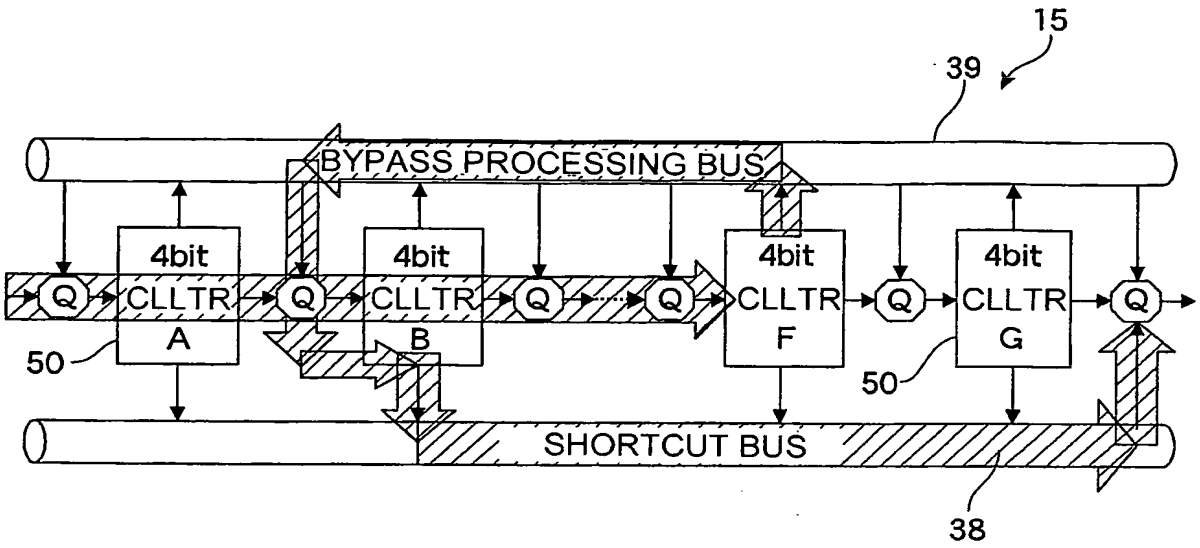

15
39
BYPASS PROCESSING BUS
4bit
CLLTR
A
4bit
CLLTR
B
4bit
CLLTR
F
4bit
CLLTR
G
Q
50
50
SHORTCUT BUS
38

FIG.37

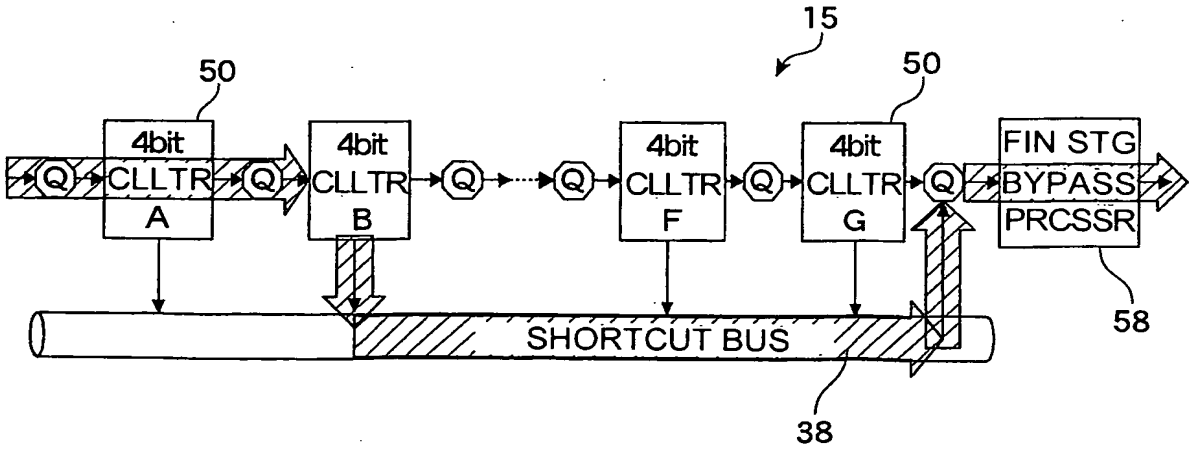

15
50
50
4bit
CLLTR
A
4bit
CLLTR
B
4bit
CLLTR
F
4bit
CLLTR
G
Q
FIN STG
BYPASS
PRCSSR
58
SHORTCUT BUS
38

FIG.38

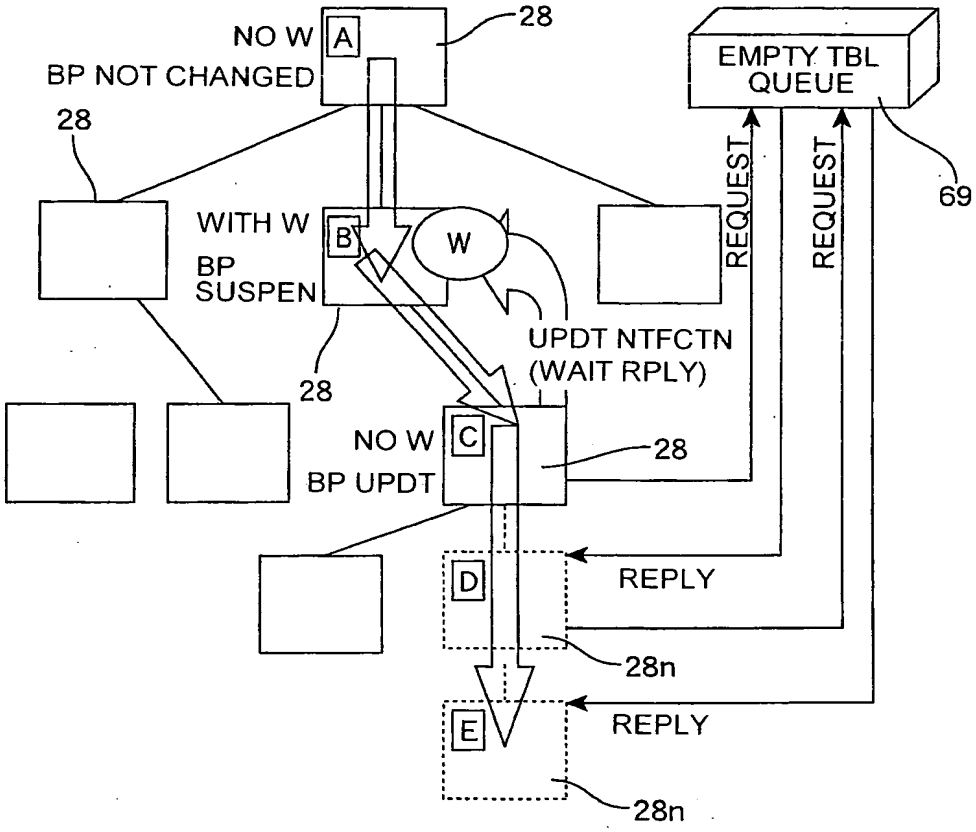

NO W
A
28
BP NOT CHANGED
EMPTY TBL QUEUE
28
69
REQUEST
REQUEST
WITH W
B
W
BP SUSPEN
UPDT NTFCTN (WAIT RPLY)
28
NO W
C
28
BP UPDT
D
REPLY
28n
E
REPLY
28n

FIG.39

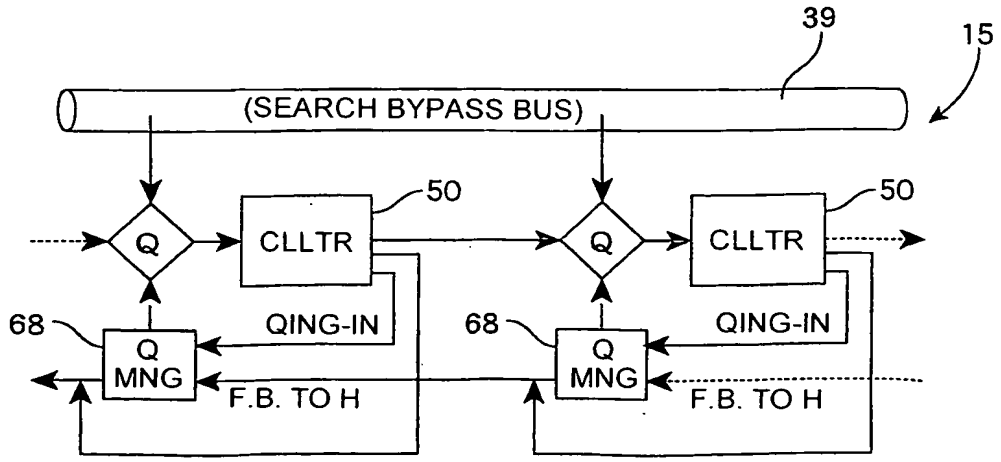

39
15
(SEARCH BYPASS BUS)
Q
CLLTR
50
Q
CLLTR
50
68
Q MNG
QING-IN
F.B. TO H
68
Q MNG
QING-IN
F.B. TO H

FIG.40

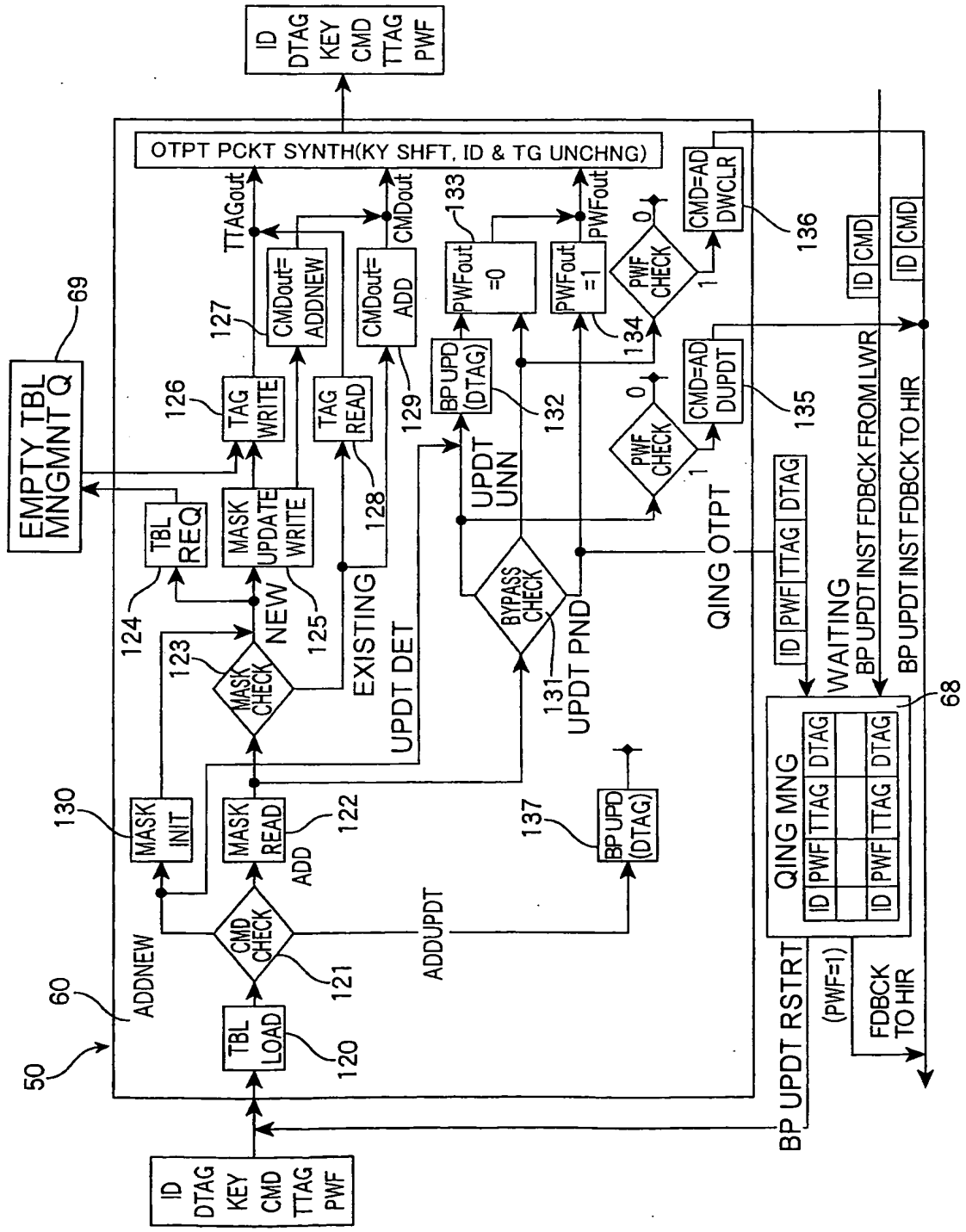

ID DTAG KEY CMD TTAG PWF
OTPT PCKT SYNTH(KY SHFT, ID & TG UNCHNG)
ID DTAG KEY CMD TTAG PWF
EMPTY TBL MNGMNT Q
69
TBL REQ
124
MASK UPDATE WRITE
125
TAG WRITE
126
TAG READ
129
CMDout= ADDNEW
127
CMDout= ADD
CMDout
TTAGout
PWFout =0
PWFout =1
PWFout
133
BP UPD (DTAG)
132
PWF CHECK
134
CMD=AD DWCLR
136
CMD=AD DUPDT
135
UPDT UNN
BYPASS CHECK
131
UPDT PND
MASK CHECK
123
NEW
EXISTING
UPDT DET
MASK INIT
130
MASK READ
122
ADD
BP UPD (DTAG)
137
CMD CHECK
121
ADDUPDT
ADDNEW
60
TBL LOAD
120
50
QING OTPT
ID PWF TTAG DTAG
WAITING
BP UPDT INST FDBCK FROM LWR
BP UPDT INST FDBCK TO HIR
ID CMD
ID CMD
QING MNG
ID PWF TTAG DTAG
ID PWF TTAG DTAG
68
BP UPDT RSTRT
(PWF=1)
FDBCK TO HIR

FIG.41

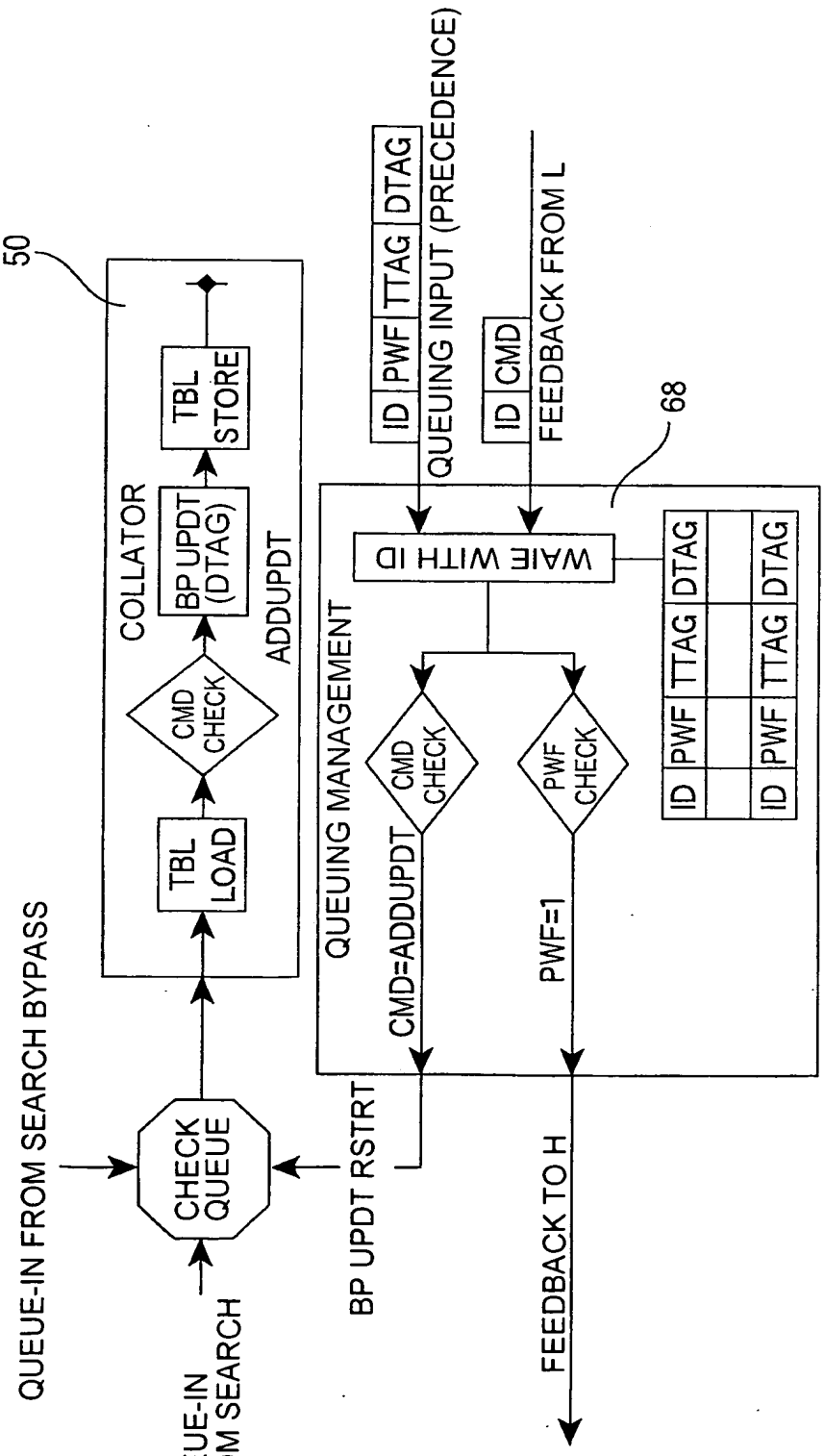

50
COLLATOR
TBL LOAD
CMD CHECK
BP UPDT (DTAG)
TBL STORE
ADDUPDT
QUEUE-IN FROM SEARCH BYPASS
QUEUE-IN FROM SEARCH
CHECK QUEUE
BP UPDT RSTRT
QUEUING MANAGEMENT
ID PWF TTAG DTAG
QUEUING INPUT (PRECEDENCE)
ID CMD
FEEDBACK FROM L
68
WAIE WITH ID
CMD CHECK
PWF CHECK
CMD=ADDUPDT
PWF=1
FEEDBACK TO H

FIG.42

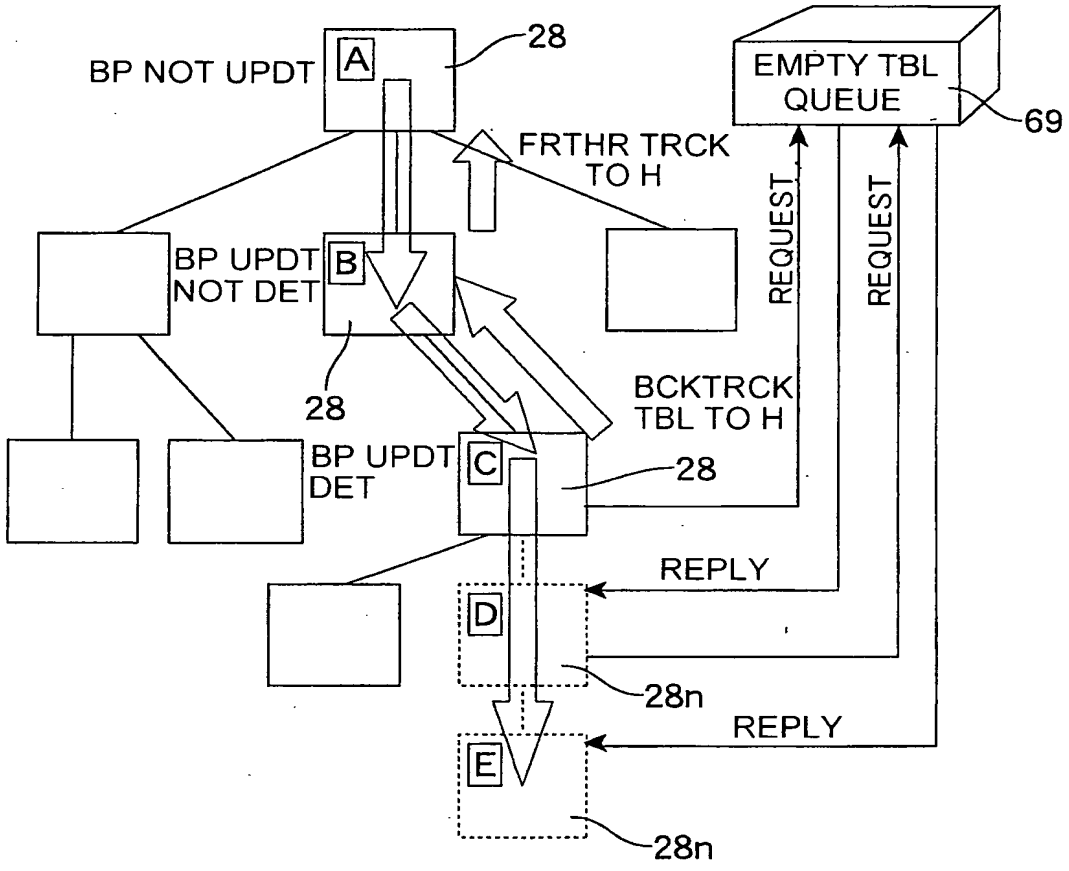

BP NOT UPDT
A
28
EMPTY TBL QUEUE
69
FRTHR TRCK TO H
REQUEST
REQUEST
BP UPDT NOT DET
B
28
BCKTRCK TBL TO H
BP UPDT DET
C
28
REPLY
D
28n
REPLY
E
28n

FIG.43

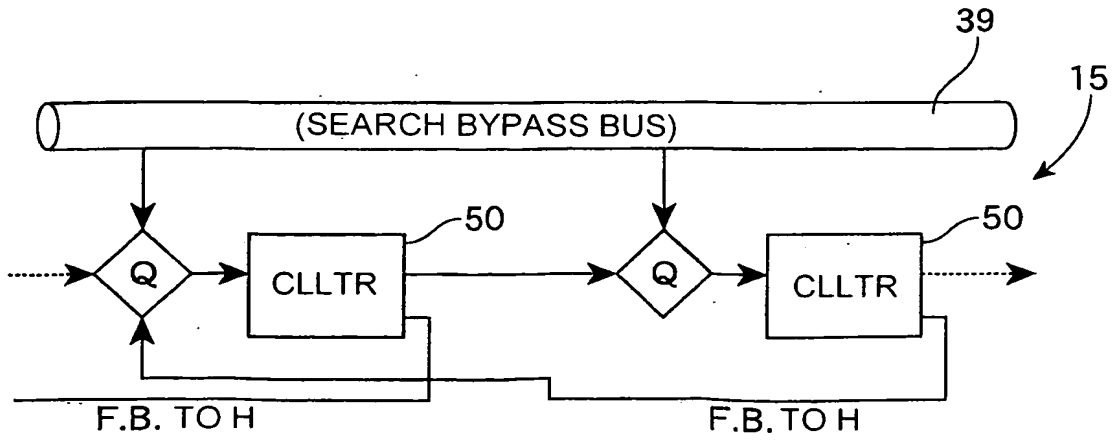

39
15
(SEARCH BYPASS BUS)
Q
CLLTR
50
Q
CLLTR
50
F.B. TO H
F.B. TO H

FIG.44

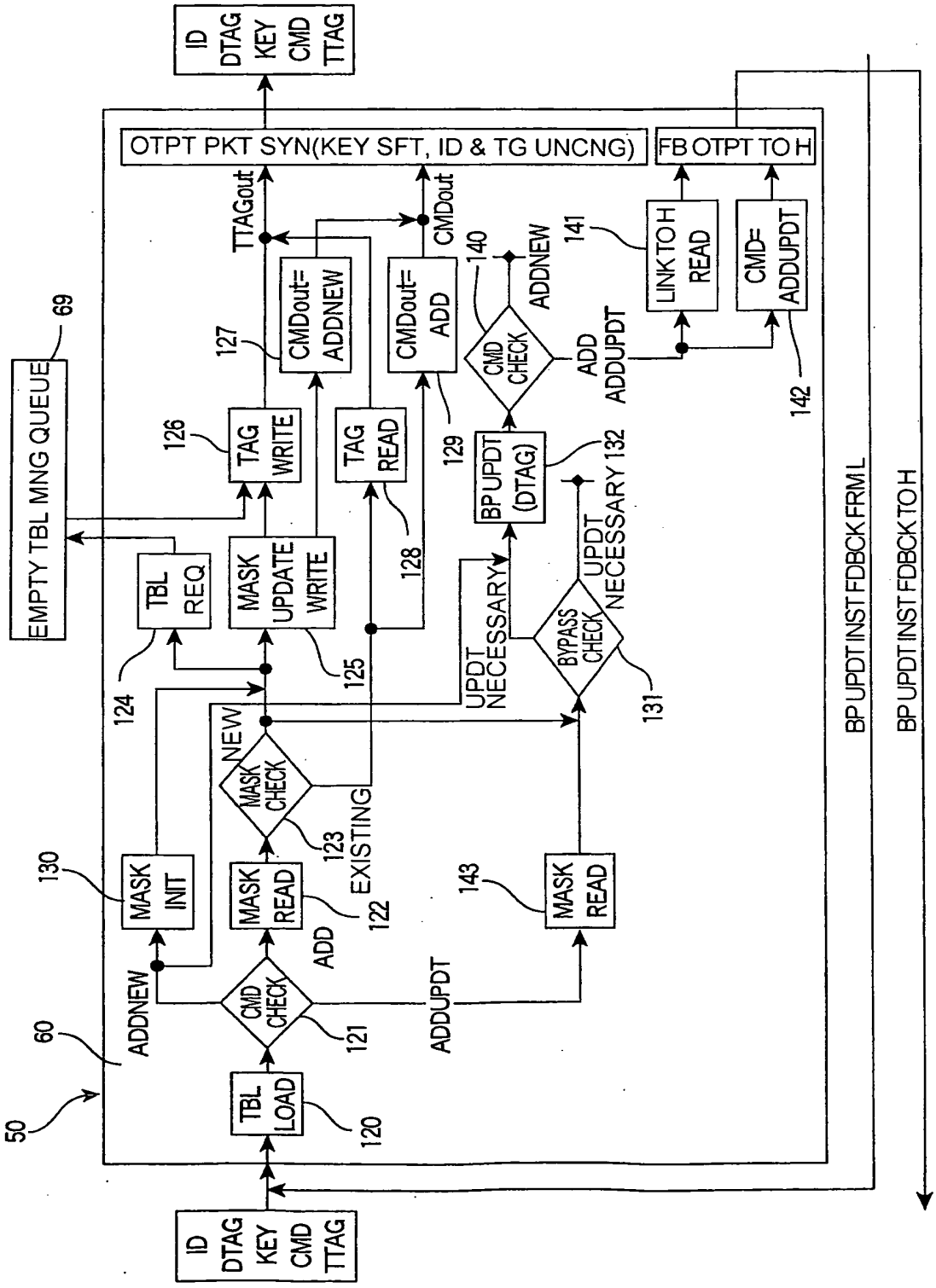

ID DTAG KEY CMD TTAG
OTPT PKT SYN(KEY SFT, ID & TG UNCNG)
FB OTPT TO H
TTAGout
CMDout
CMDout= ADDNEW
CMDout= ADD
ADDNEW
LINK TO H READ
CMD= ADDUPDT
CMD CHECK
ADD
ADDUPDT
EMPTY TBL MNG QUEUE
TAG WRITE
TAG READ
BP UPDT (DTAG)
TBL REQ
MASK UPDATE WRITE
UPDT NECESSARY
BYPASS CHECK
UPDT NECESSARY
MASK CHECK
NEW
EXISTING
MASK INIT
MASK READ
MASK READ
ADDNEW
ADD
ADDUPDT
CMD CHECK
TBL LOAD
BP UPDT INST FDBCK FRM L
BP UPDT INST FDBCK TO H
ID DTAG KEY CMD TTAG
50
60
69
120
121
122
123
124
125
126
127
128
129
130
131
132
140
141
142
143

FIG.45

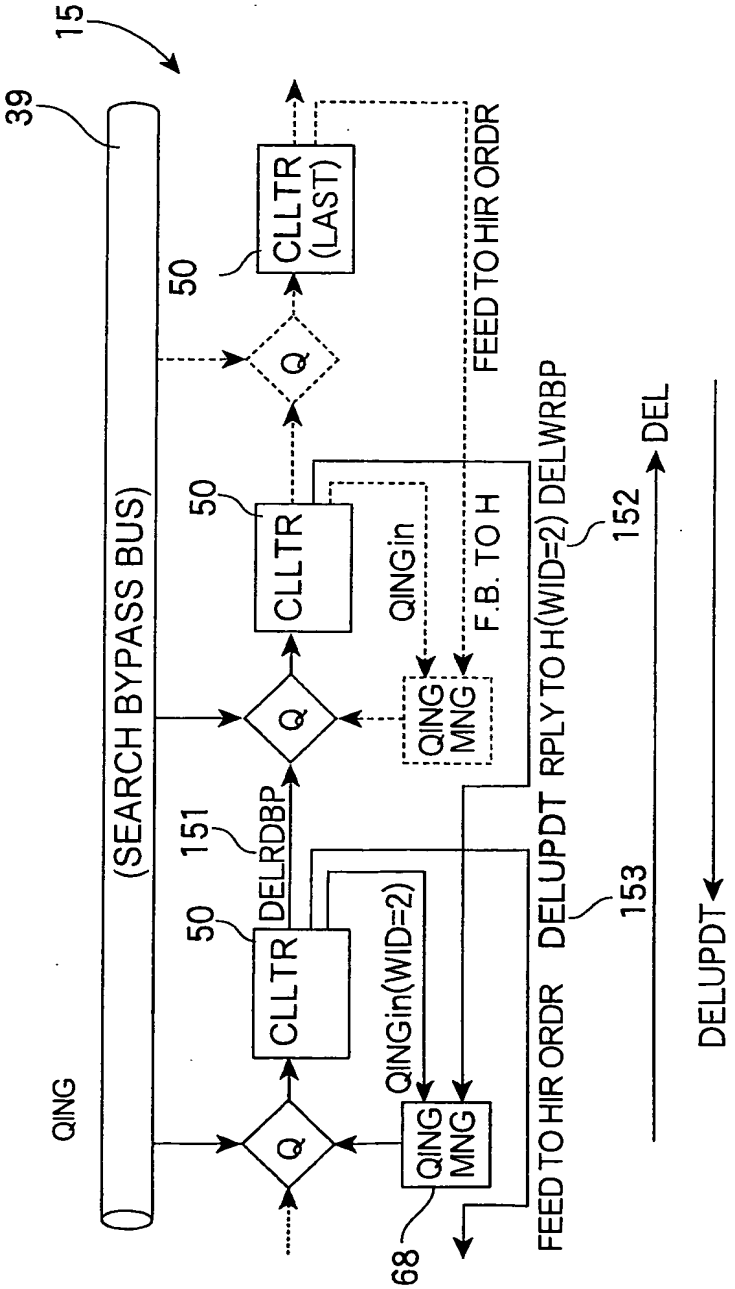

15
39
(SEARCH BYPASS BUS)
QING
50
CLLTR
(LAST)
Q
FEED TO HIR ORDR
50
CLLTR
QINGin
F.B. TO H
Q
QING
MNG
151
DELRDBP
50
CLLTR
QINGin(WID=2)
Q
QING
MNG
68
FEED TO HIR ORDR
DELUPDT
RPLY TO H(WID=2) DELWRBP
152
DEL
153
DELUPDT

FIG.46

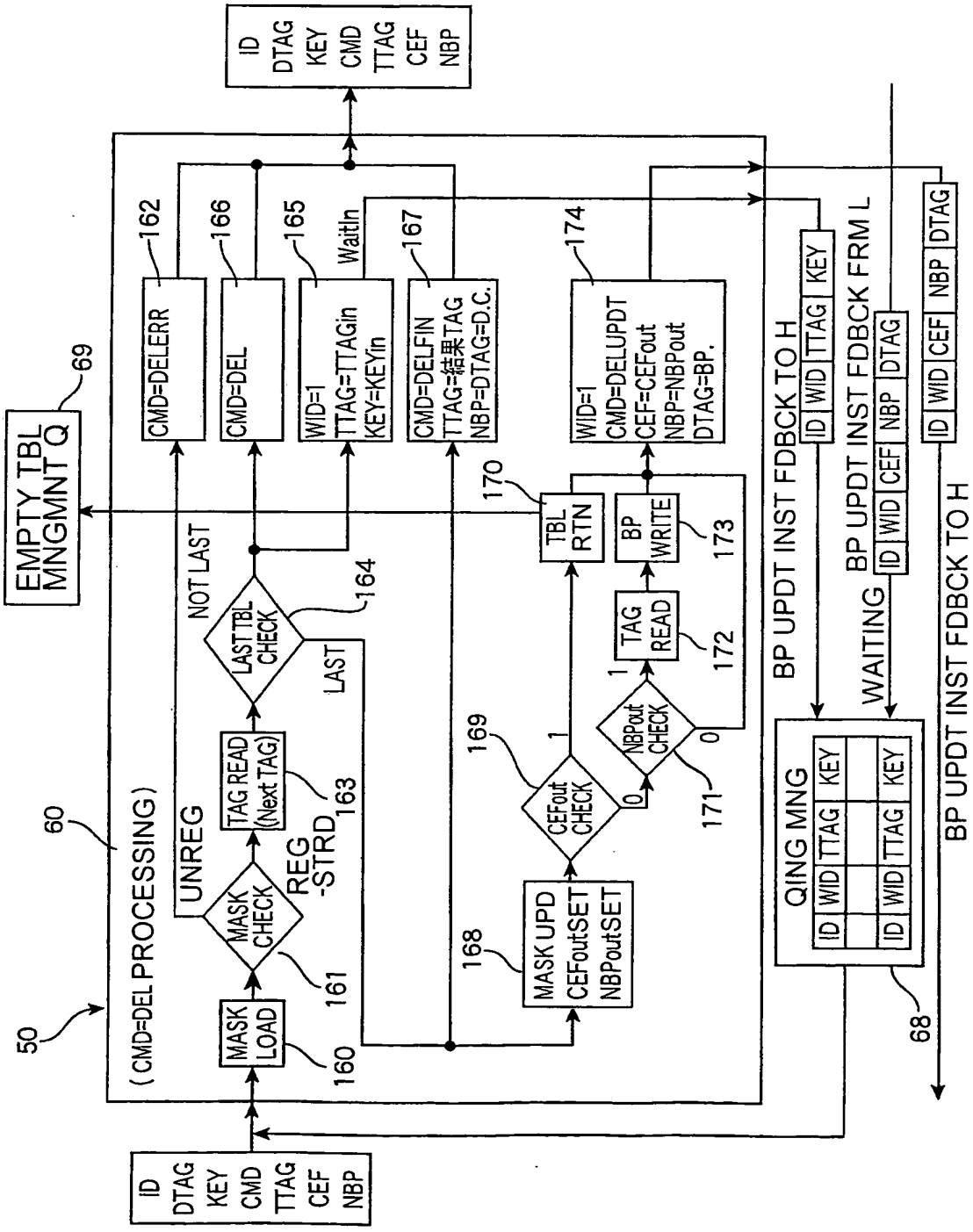

ID DTAG KEY CMD TTAG CEF NBP
50
(CMD=DEL PROCESSING)
60
MASK LOAD
160
MASK CHECK
161
UNREG
REG -STRD
TAG READ (Next TAG)
163
LAST TBL CHECK
164
NOT LAST
LAST
EMPTY TBL MNGMNT Q
69
CMD=DELERR
162
CMD=DEL
166
WID=1 TTAG=TTAGin KEY=KEYin
165
WaitIn
CMD=DELFIN TTAG=結果TAG NBP=DTAG=D.C.
167
MASK UPD CEFoutSET NBPoutSET
168
CEFout CHECK
169
TBL RTN
170
WID=1 CMD=DELUPDT CEF=CEFout NBP=NBPout DTAG=BP.
174
NBPout CHECK
171
TAG READ
172
BP WRITE
173
BP UPDT INST FDBCK TO H
ID WID TTAG KEY
WAITING
QING MNG
ID WID TTAG KEY
BP UPDT INST FDBCK FRM L
ID WID CEF NBP DTAG
68
BP UPDT INST FDBCK TO H
ID WID CEF NBP DTAG

FIG.47

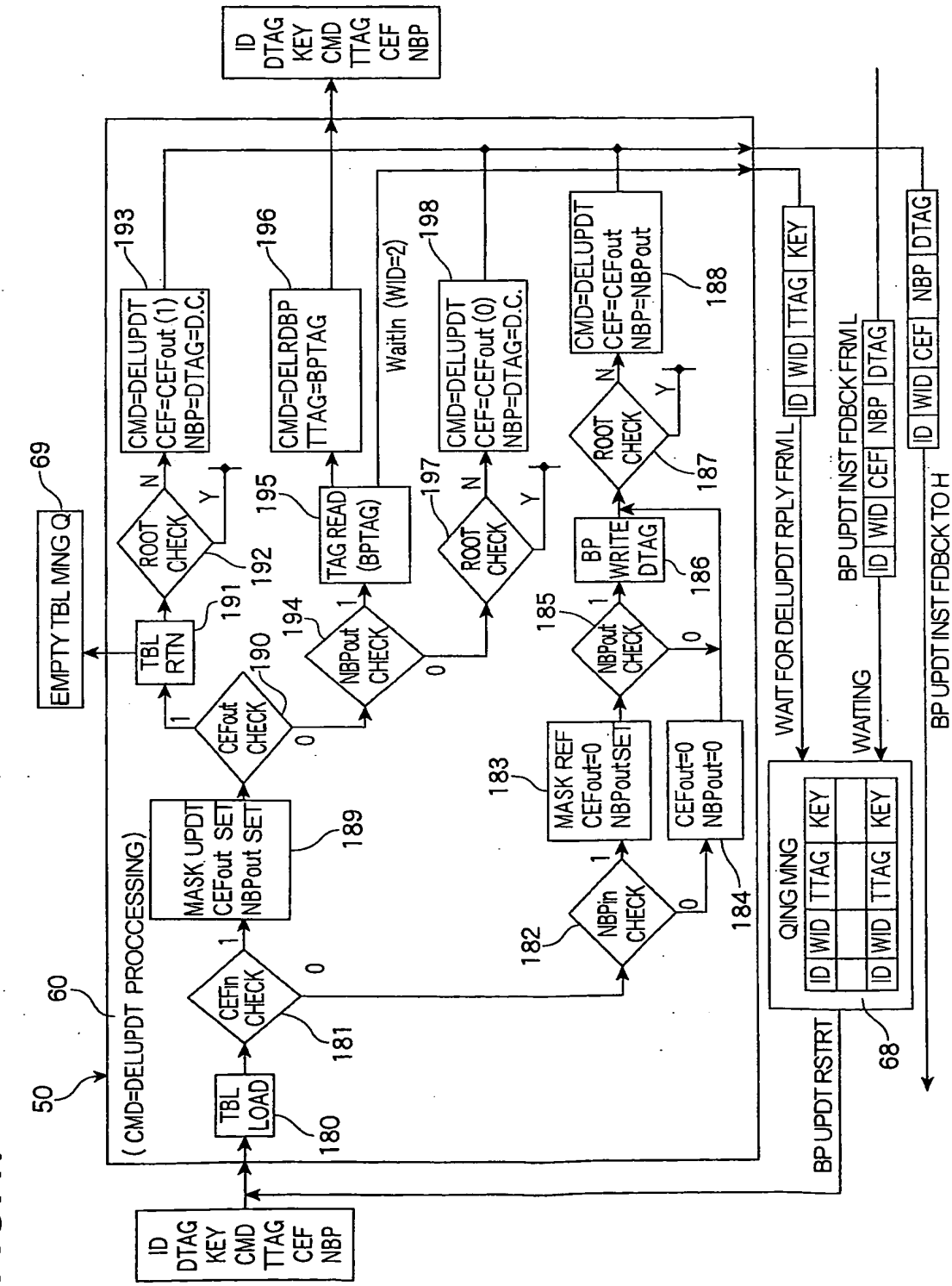

ID DTAG KEY CMD TTAG CEF NBP
50
60
(CMD=DELUPDT PROCCESSING)
TBL LOAD
180
CEFin CHECK
181
MASK UPDT CEFout SET NBPout SET
189
CEFout CHECK
190
TBL RTN
191
ROOT CHECK
192
CMD=DELUPDT CEF=CEFout (1) NBP=DTAG=D.C.
193
NBPout CHECK
194
TAG READ (BPTAG)
195
CMD=DELRDBP TTAG=BPTAG
196
ROOT CHECK
197
CMD=DELUPDT CEF=CEFout (0) NBP=DTAG=D.C.
198
WaitIn (WID=2)
EMPTY TBL MNG Q
69
NBPin CHECK
182
MASK REF CEFout=0 NBPoutSET
183
CEFout=0 NBPout=0
184
NBPout CHECK
185
BP WRITE DTAG
186
ROOT CHECK
187
CMD=DELUPDT CEF=CEFout NBP=NBPout
188
WAIT FOR DELUPDT RPLY FRM L
ID WID TTAG KEY
BP UPDT INST FDBCK FRM L
ID WID CEF NBP DTAG
WAITING
QING MING
ID WID TTAG KEY
ID WID TTAG KEY
68
BP UPDT RSTRT
BP UPDT INST FDBCK TO H
ID WID CEF NBP DTAG
ID DTAG KEY CMD TTAG CEF NBP

FIG.48

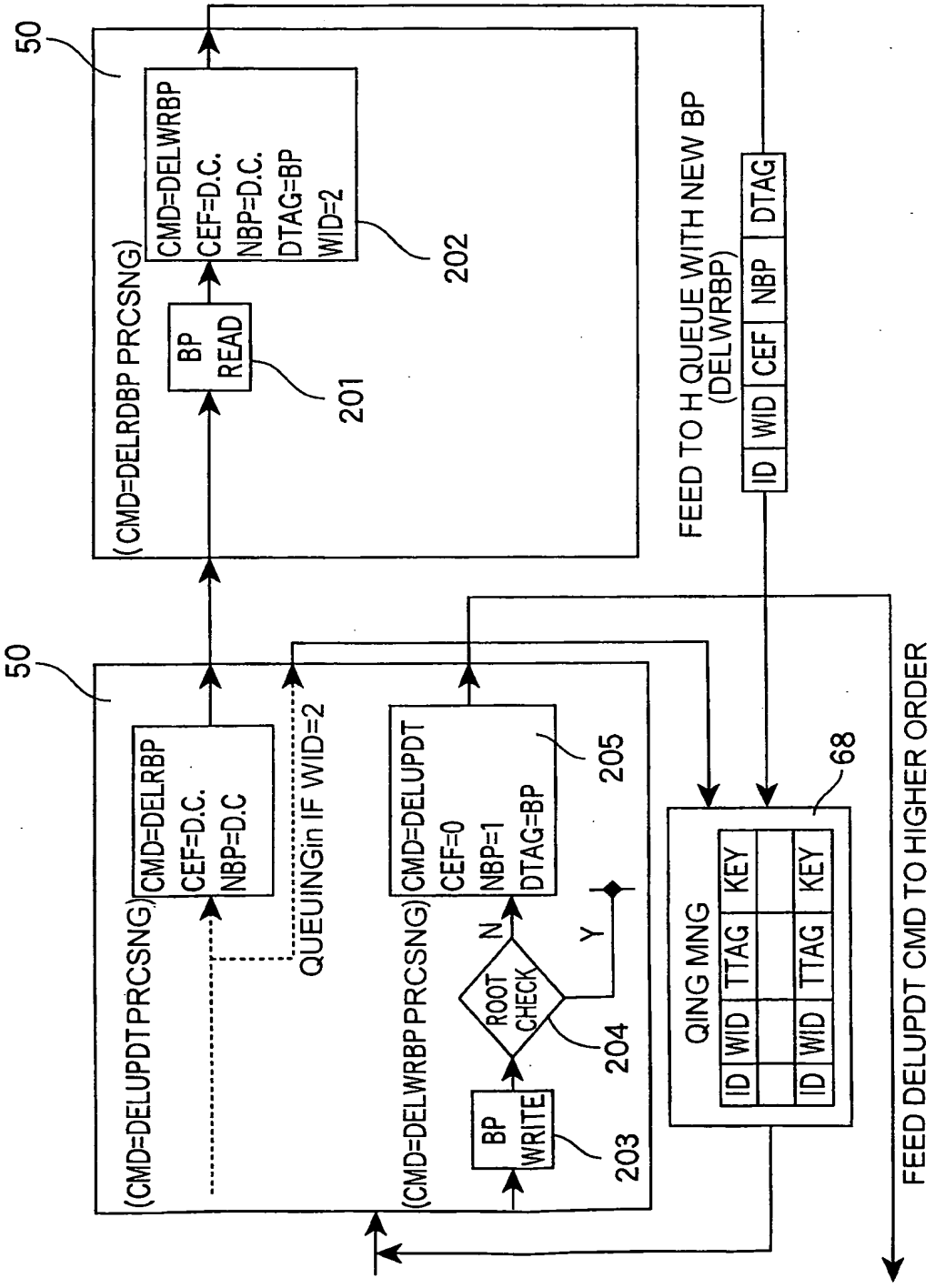

50
(CMD=DELRDBP PRCSNG)
BP READ
201
CMD=DELWRBP
CEF=D.C.
NBP=D.C.
DTAG=BP
WID=2
202
FEED TO H QUEUE WITH NEW BP (DELWRBP)
ID
WID
CEF
NBP
DTAG
50
(CMD=DELUPDT PRCSNG)
CMD=DELRBP
CEF=D.C.
NBP=D.C
QUEUINGin IF WID=2
(CMD=DELWRBP PRCSNG)
CMD=DELUPDT
CEF=0
NBP=1
DTAG=BP
205
ROOT CHECK
N
Y
204
BP WRITE
203
QING MNG
ID
WID
TTAG
KEY
68
FEED DELUPDT CMD TO HIGHER ORDER

FIG.49

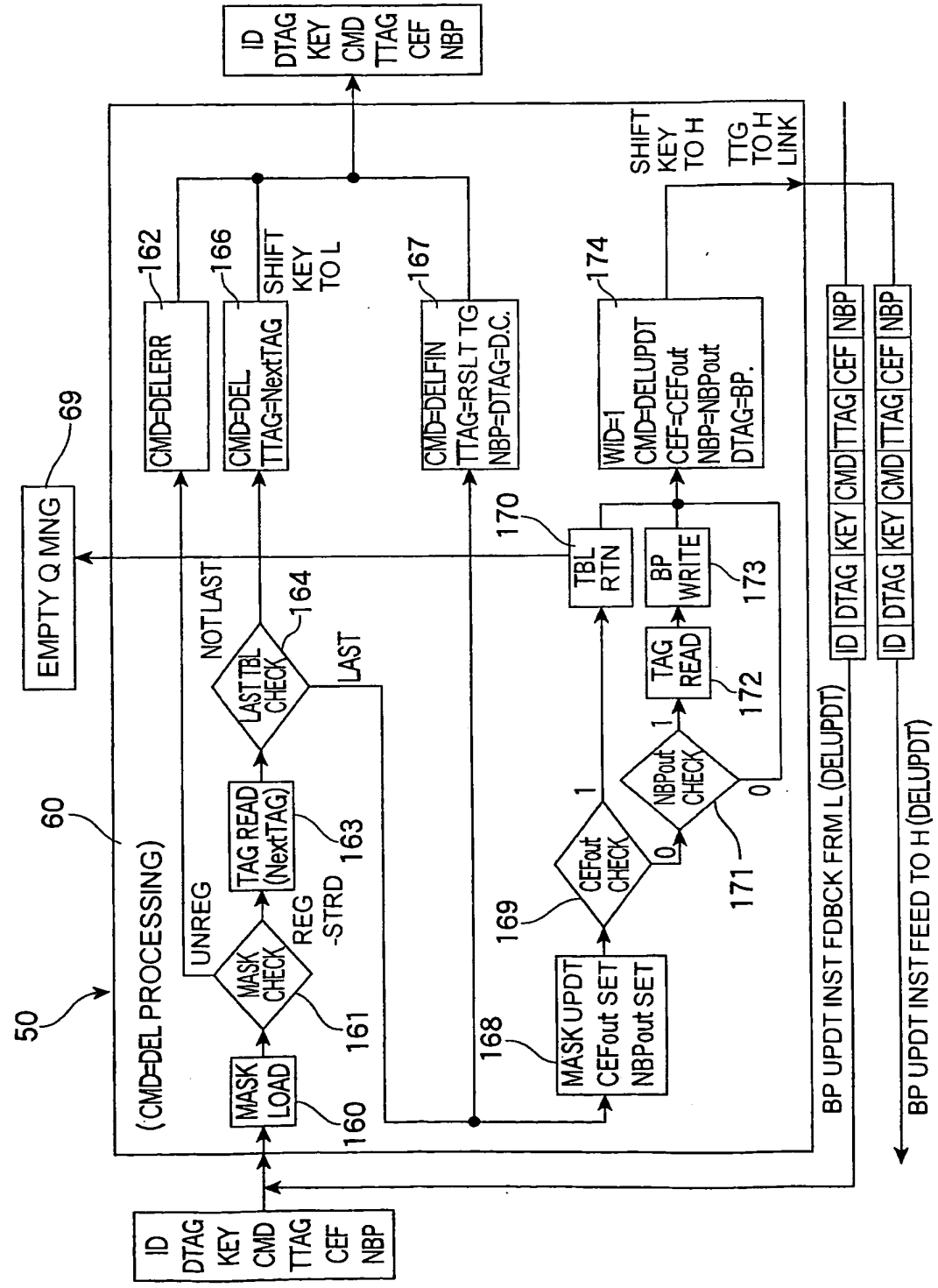

ID DTAG KEY CMD TTAG CEF NBP
50
60
(CMD=DEL PROCESSING)
MASK LOAD
160
MASK CHECK
161
UNREG
REG
-STRD
TAG READ (NextTAG)
163
LAST TBL CHECK
164
NOT LAST
LAST
EMPTY Q MNG
69
CMD=DELERR
162
CMD=DEL TTAG=NextTAG
166
SHIFT KEY TO L
CMD=DELFIN TTAG=RSLT TG NBP=DTAG=D.C.
167
168
MASK UPDT CEFout SET NBPout SET
CEFout CHECK
169
1
0
TBL RTN
170
WID=1 CMD=DELUPDT CEF=CEFout NBP=NBPout DTAG=BP.
174
BP WRITE
173
TAG READ
172
NBPout CHECK
171
SHIFT KEY TO H
TTG TO H LINK
ID DTAG KEY CMD TTAG CEF NBP
BP UPDT INST FDBCK FRM L (DELUPDT)
BP UPDT INST FEED TO H (DELUPDT)

FIG.50

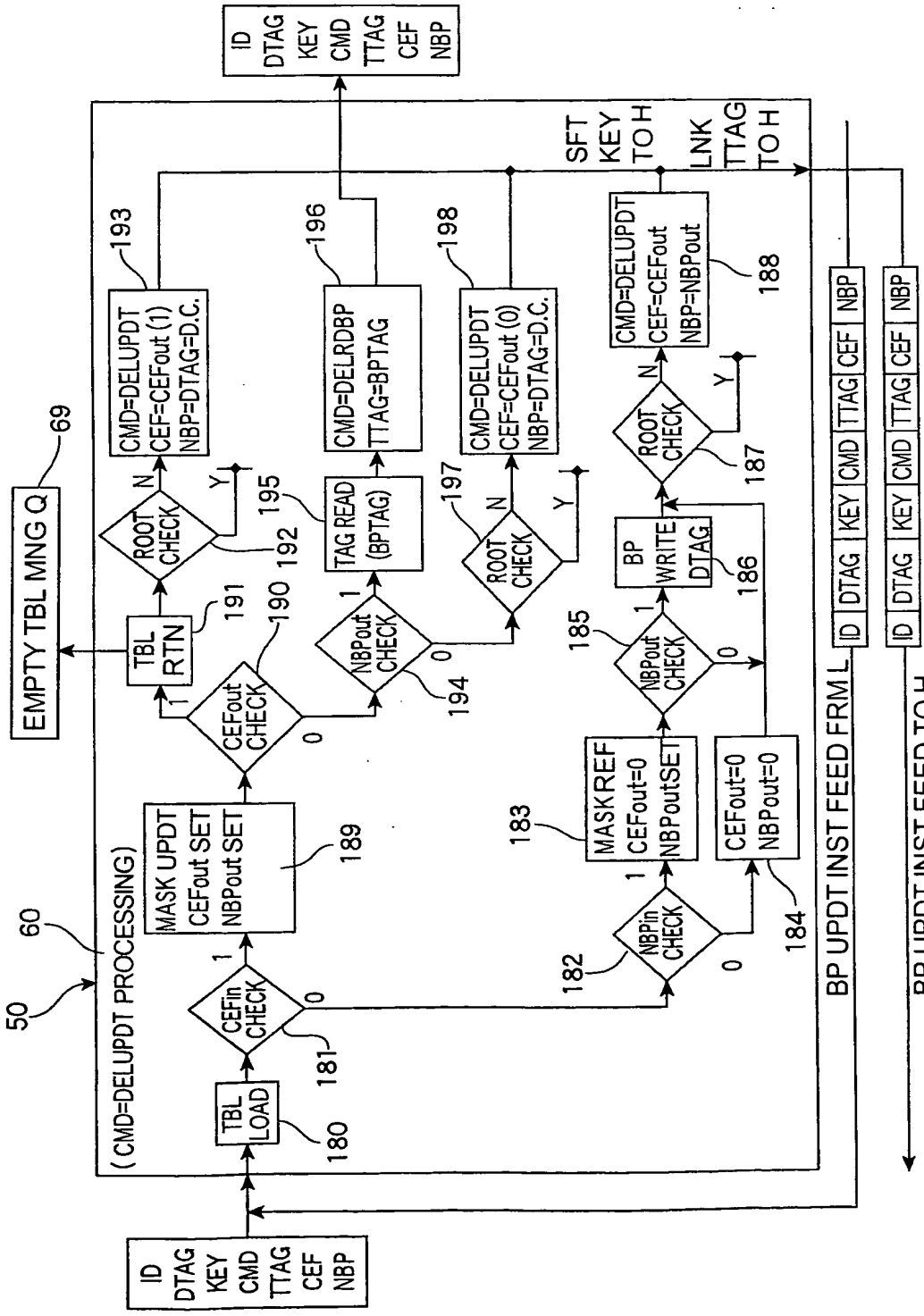

ID DTAG KEY CMD TTAG CEF NBP
(CMD=DELUPDT PROCESSING)
50
60
TBL LOAD
180
CEFin CHECK
181
MASK UPDT CEFout SET NBPout SET
189
CEFout CHECK
190
TBL RTN
191
EMPTY TBL MNG Q
69
ROOT CHECK
192
CMD=DELUPDT CEF=CEFout (1) NBP=DTAG=D.C.
193
TAG READ (BPTAG)
195
CMD=DELRDBP TTAG=BPTAG
196
NBPout CHECK
194
ROOT CHECK
197
CMD=DELUPDT CEF=CEFout (0) NBP=DTAG=D.C.
198
NBPin CHECK
182
MASK REF CEFout=0 NBPoutSET
183
NBPout CHECK
185
BP WRITE DTAG
186
ROOT CHECK
187
CMD=DELUPDT CEF=CEFout NBP=NBPout
188
CEFout=0 NBPout=0
184
SFT KEY TO H
LNK TTAG TO H
ID DTAG KEY CMD TTAG CEF NBP
BP UPDT INST FEED FRM L
BP UPDT INST FEED TO H

FIG.51

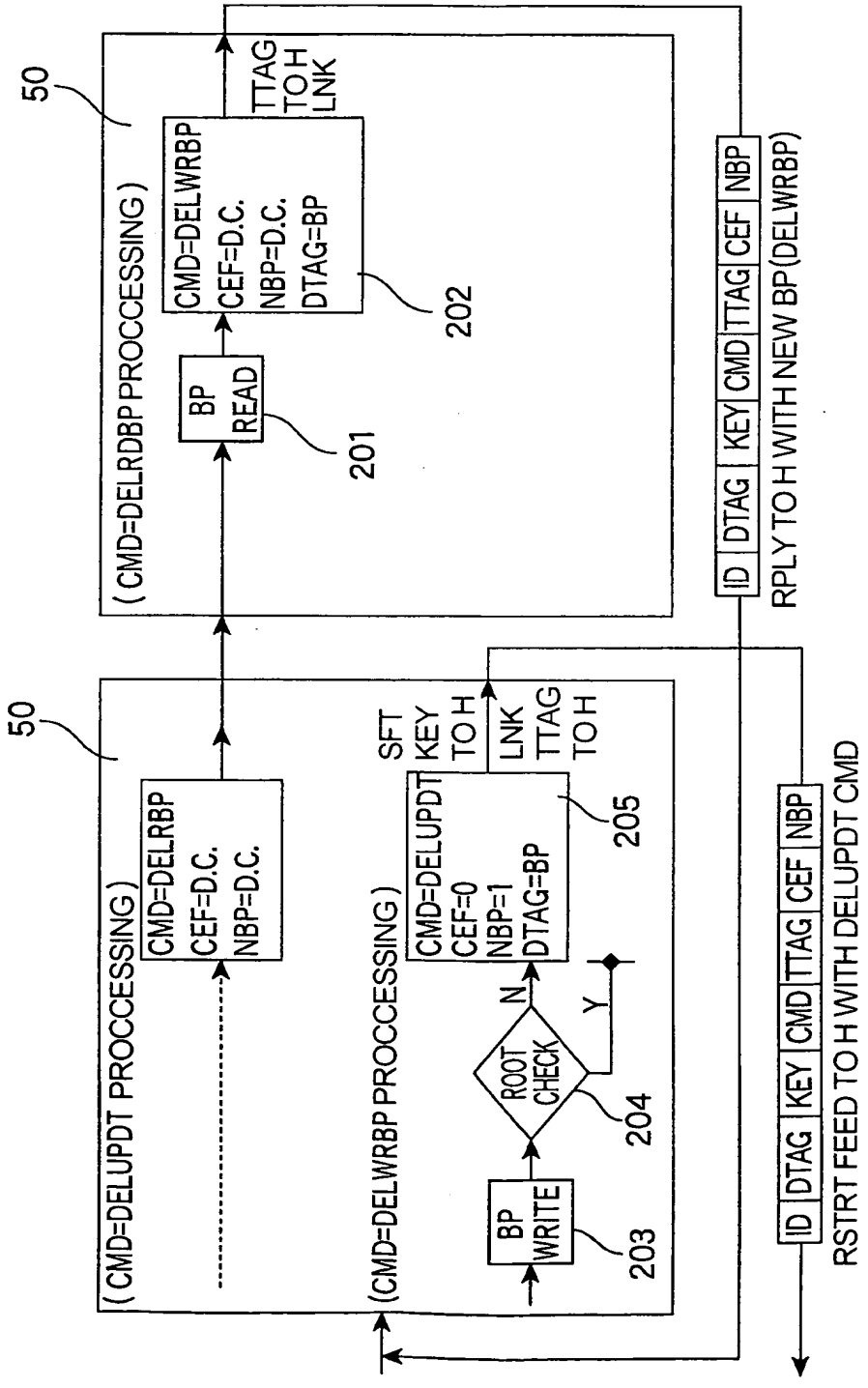

50
(CMD=DELRDBP PROCCESSING)
BP READ
201
CMD=DELWRBP
CEF=D.C.
NBP=D.C.
DTAG=BP
202
TTAG TO H LNK
ID DTAG KEY CMD TTAG CEF NBP
RPLY TO H WITH NEW BP(DELWRBP)
50
(CMD=DELUPDT PROCCESSING)
CMD=DELRBP
CEF=D.C.
NBP=D.C.
(CMD=DELWRBP PROCCESSING)
BP WRITE
203
ROOT CHECK
204
N
Y
CMD=DELUPDT
CEF=0
NBP=1
DTAG=BP
205
SFT KEY TO H
LNK TTAG TO H
ID DTAG KEY CMD TTAG CEF NBP
RSTRT FEED TO H WITH DELUPDT CMD

FIG.52

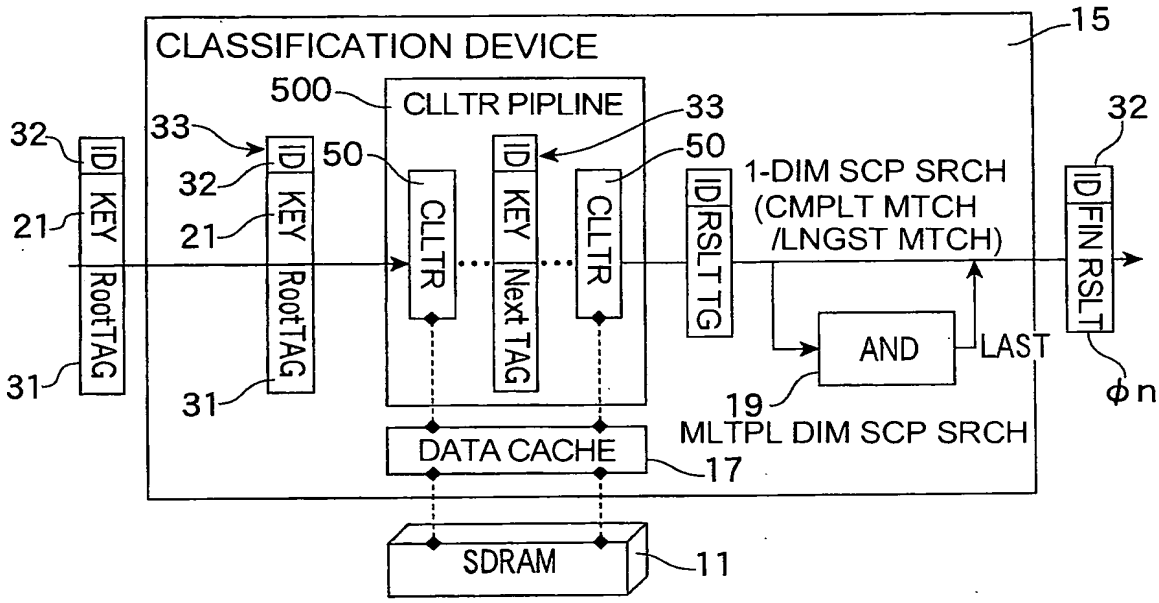
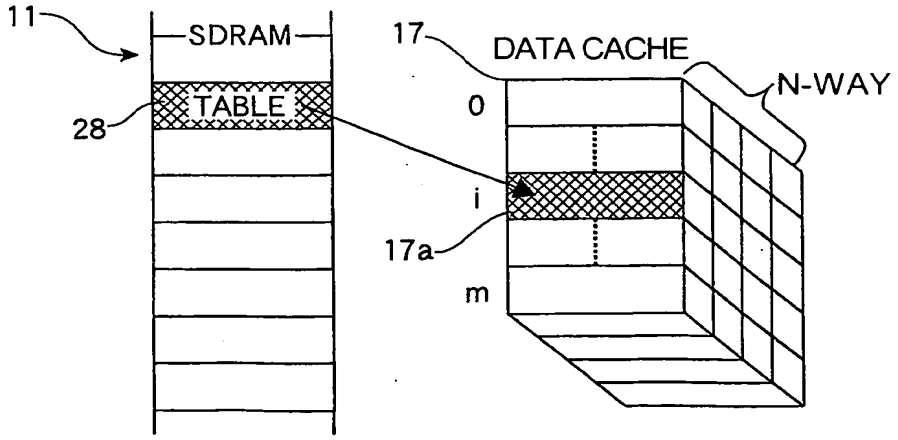

CLASSIFICATION DEVICE
15
500
CLLTR PIPLINE
33
50
32
ID
KEY
RootTAG
21
31
CLLTR
Next TAG
1-DIM SCP SRCH
(CMPLT MTCH
/LNGST MTCH)
RSLT TG
AND
LAST
19
MLTPL DIM SCP SRCH
FIN RSLT
φn
DATA CACHE
17
SDRAM
11

FIG.53


11
SDRAM
TABLE
28
17
DATA CACHE
N-WAY
0
i
17a
m

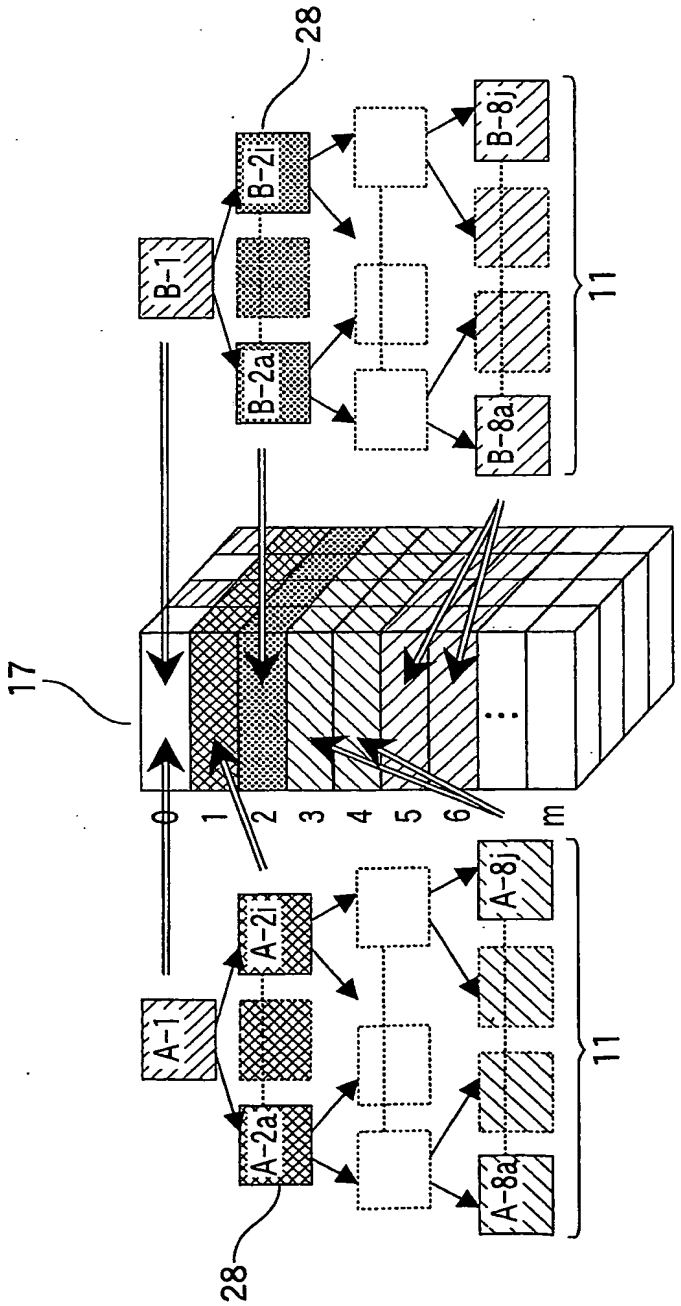


FIG.54

FIG.55

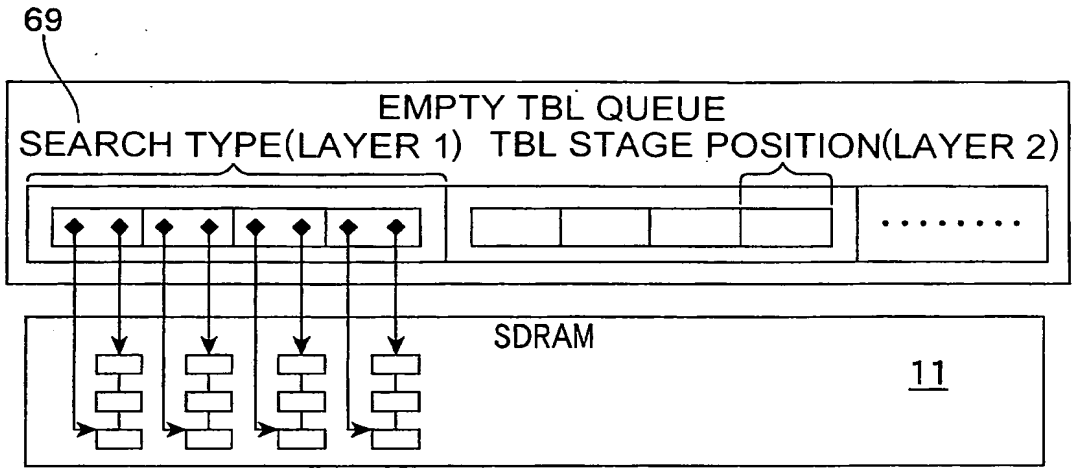
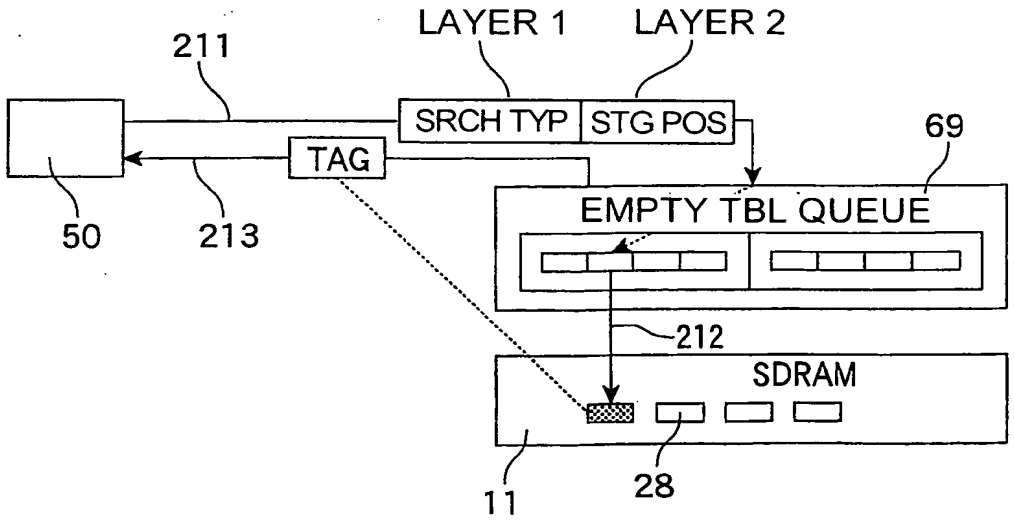

69
EMPTY TBL QUEUE
SEARCH TYPE(LAYER 1)
TBL STAGE POSITION(LAYER 2)
SDRAM
11

FIG.56


LAYER 1
LAYER 2
211
SRCH TYP
STG POS
69
TAG
50
213
EMPTY TBL QUEUE
212
SDRAM
11
28

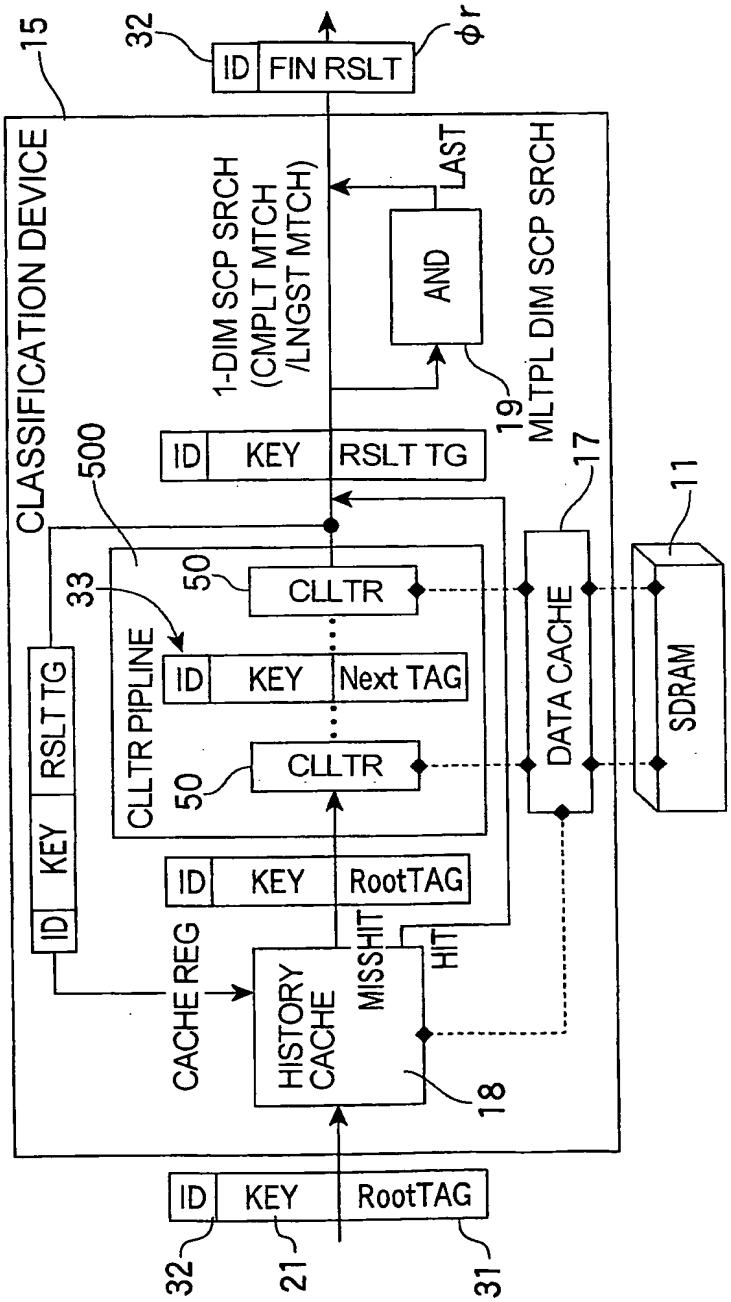
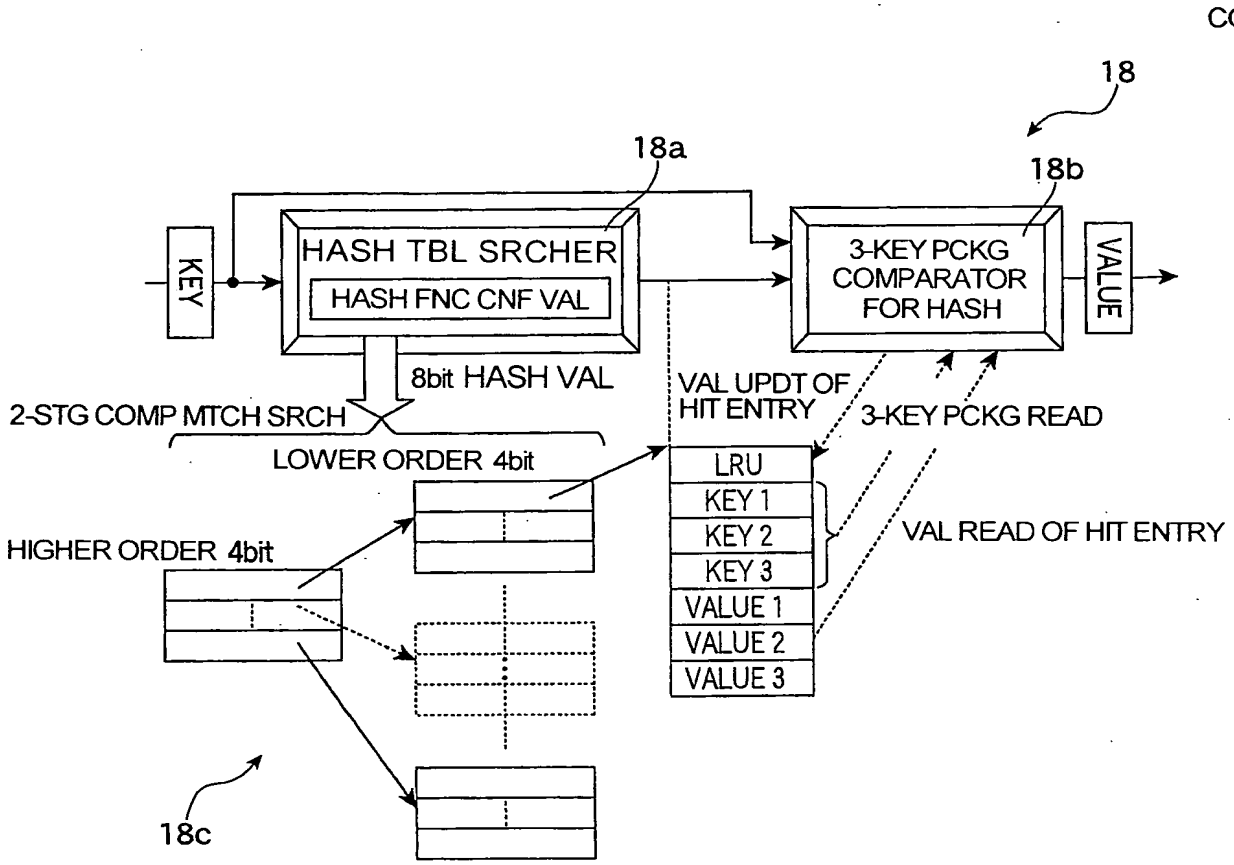

15
32
ID
FIN RSLT
φr
CLASSIFICATION DEVICE
1-DIM SCP SRCH
(CMPLT MTCH
/LNGST MTCH)
LAST
AND
19
MLTPL DIM SCP SRCH
500
ID
KEY
RSLT TG
17
11
33
50
CLLTR
CLLTR PIPLINE
ID
KEY
Next TAG
CLLTR
50
DATA CACHE
SDRAM
ID
KEY
RSLT TG
ID
KEY
RootTAG
CACHE REG
MISSHIT
HIT
HISTORY
CACHE
18
ID
KEY
RootTAG
32
21
31

FIG.57

FIG.58


COMP
18
18a
18b
KEY
HASH TBL SRCHER
HASH FNC CNF VAL
3-KEY PCKG COMPARATOR FOR HASH
VALUE
8bit HASH VAL
2-STG COMP MTCH SRCH
LOWER ORDER 4bit
VAL UPDT OF HIT ENTRY
3-KEY PCKG READ
LRU
KEY 1
KEY 2
KEY 3
VALUE 1
VALUE 2
VALUE 3
VAL READ OF HIT ENTRY
HIGHER ORDER 4bit
18c

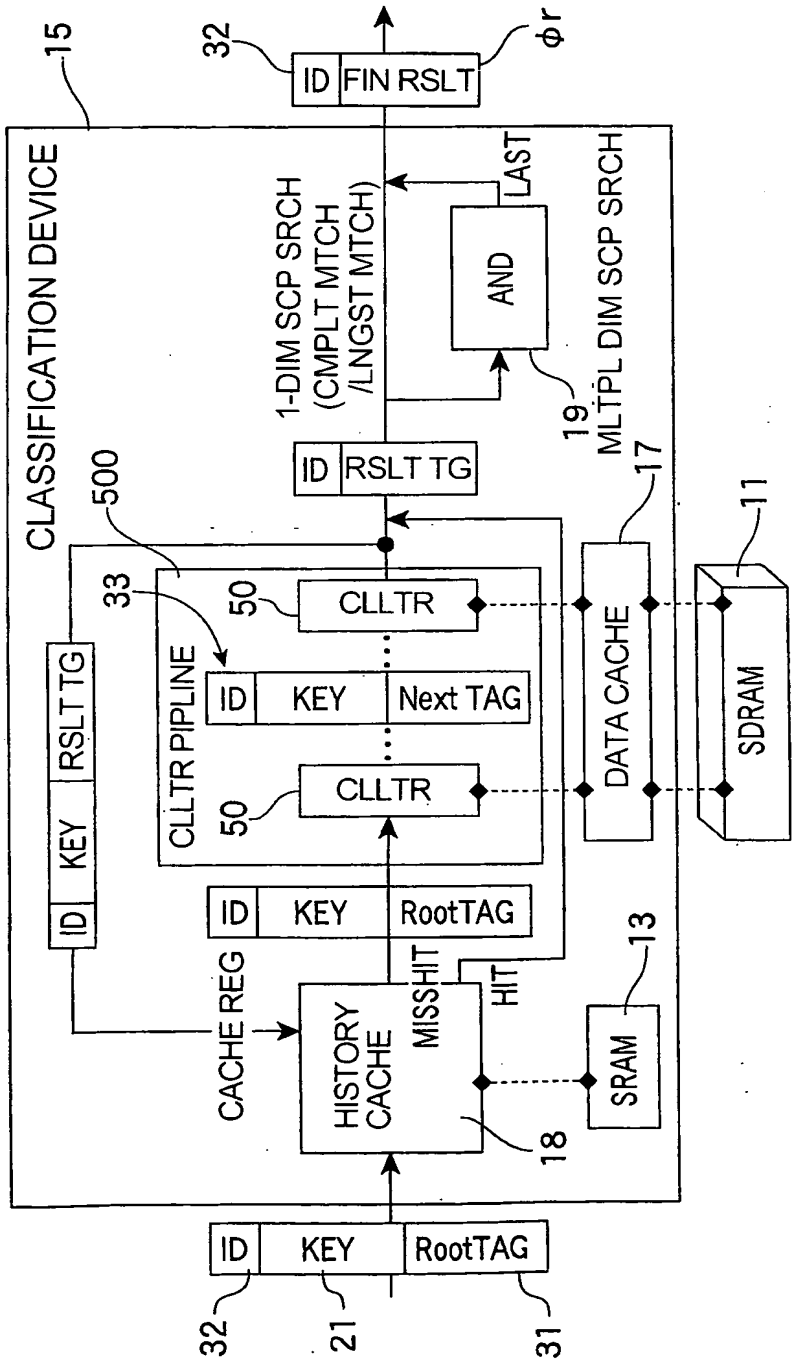

15
CLASSIFICATION DEVICE
32
ID
FIN RSLT
φr
1-DIM SCP SRCH
(CMPLT MTCH
/LNGST MTCH)
LAST
AND
19
MLTPL DIM SCP SRCH
ID
RSLT TG
500
17
11
33
50
CLLTR
ID
KEY
Next TAG
CLLTR PIPLINE
50
CLLTR
DATA CACHE
SDRAM
RSLT TG
KEY
ID
ID
KEY
RootTAG
13
CACHE REG
MISSHIT
HIT
HISTORY
CACHE
SRAM
18
ID
KEY
RootTAG
32
21
31

FIG.59

FIG.60

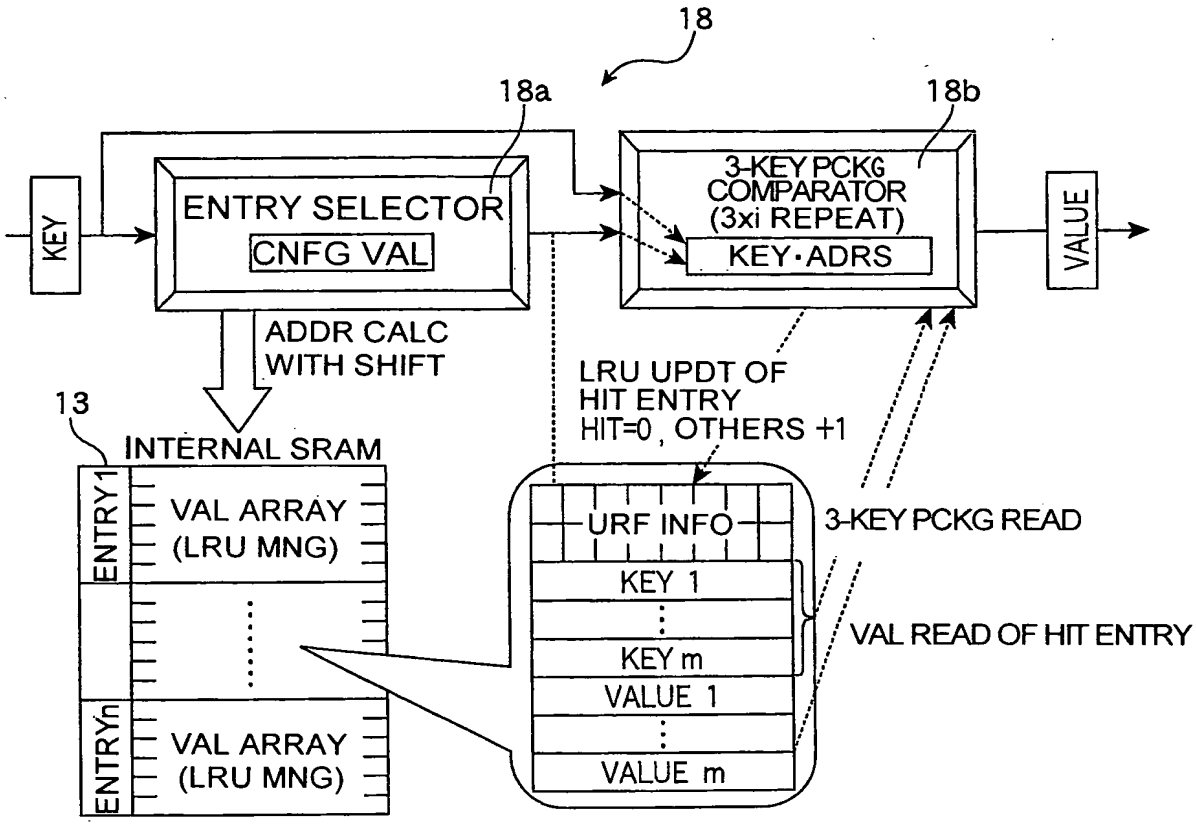

18
18a
18b
KEY
ENTRY SELECTOR
CNFG VAL
3-KEY PCKG
COMPARATOR
(3xi REPEAT)
KEY・ADRS
VALUE
ADDR CALC
WITH SHIFT
LRU UPDT OF
HIT ENTRY
HIT=0, OTHERS +1
13
INTERNAL SRAM
ENTRY 1
VAL ARRAY
(LRU MNG)
ENTRYn
VAL ARRAY
(LRU MNG)
URF INFO
KEY 1
KEY m
VALUE 1
VALUE m
3-KEY PCKG READ
VAL READ OF HIT ENTRY

FIG.61

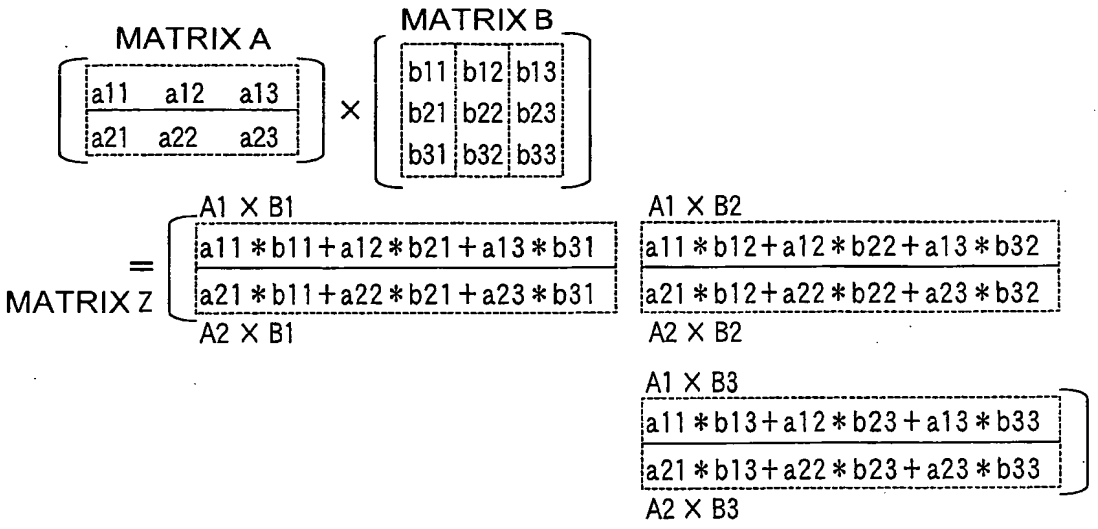


FIG.62

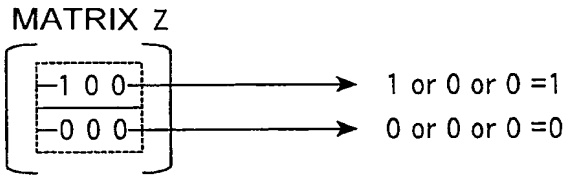


FIG.63

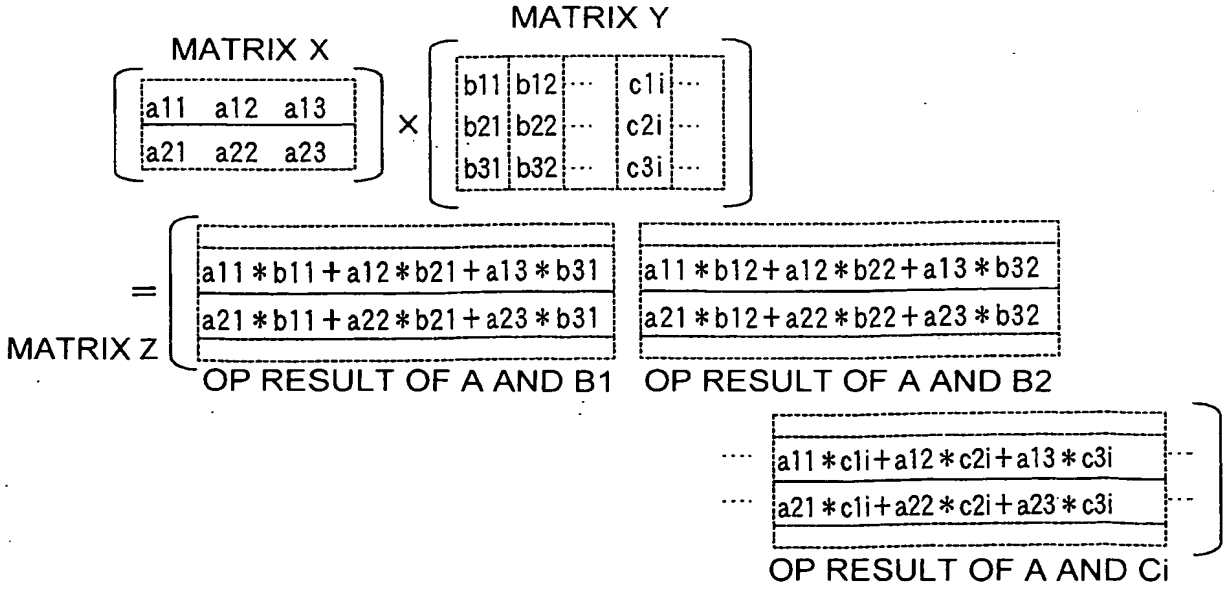


FIG.64

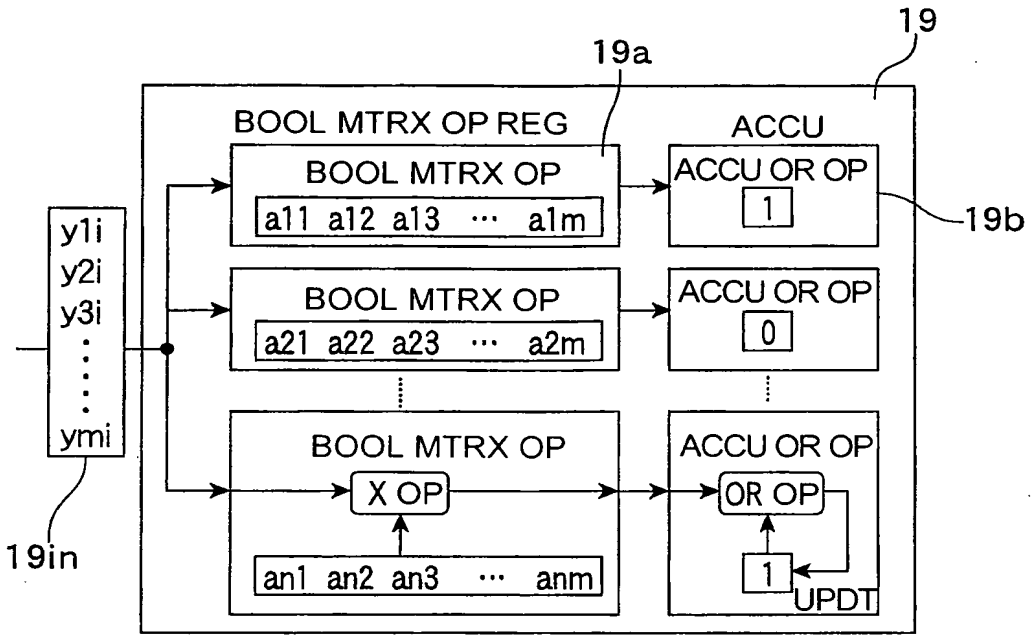

19
19a
BOOL MTRX OP REG
ACCU
BOOL MTRX OP
a11 a12 a13 ··· a1m
ACCU OR OP
1
19b
BOOL MTRX OP
a21 a22 a23 ··· a2m
ACCU OR OP
0
BOOL MTRX OP
X OP
an1 an2 an3 ··· anm
ACCU OR OP
OR OP
1
UPDT
y1i
y2i
y3i
ymi
19in

FIG.65

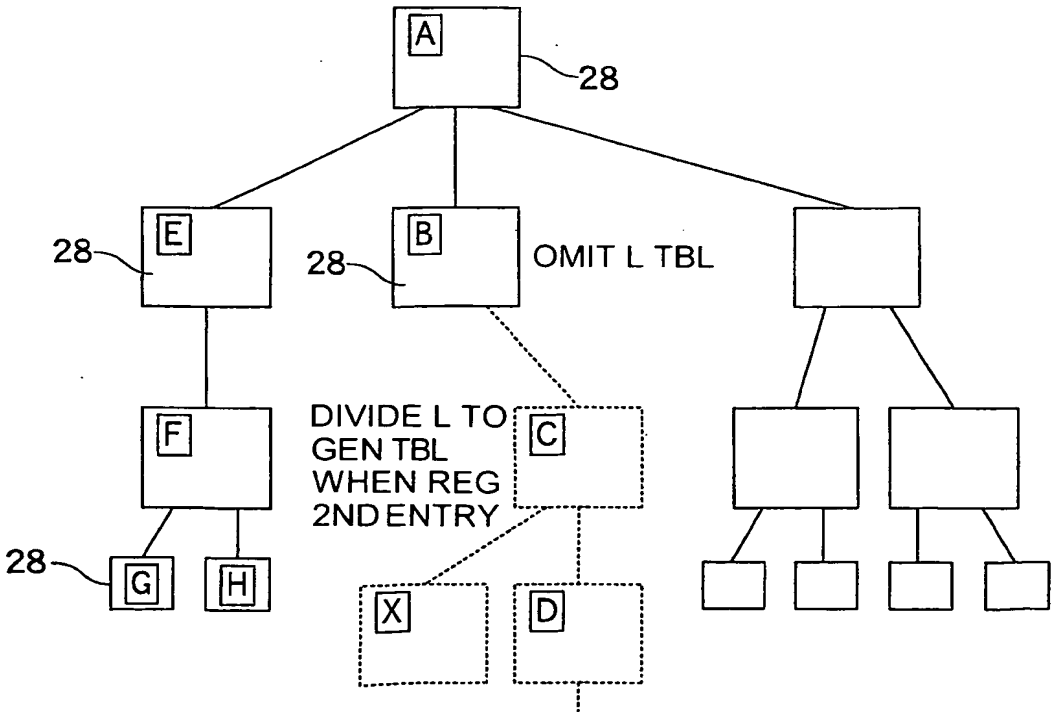

A
28
E
28
B
28
OMIT L TBL
F
DIVIDE L TO GEN TBL WHEN REG 2ND ENTRY
C
28
G
H
X
D

FIG.66

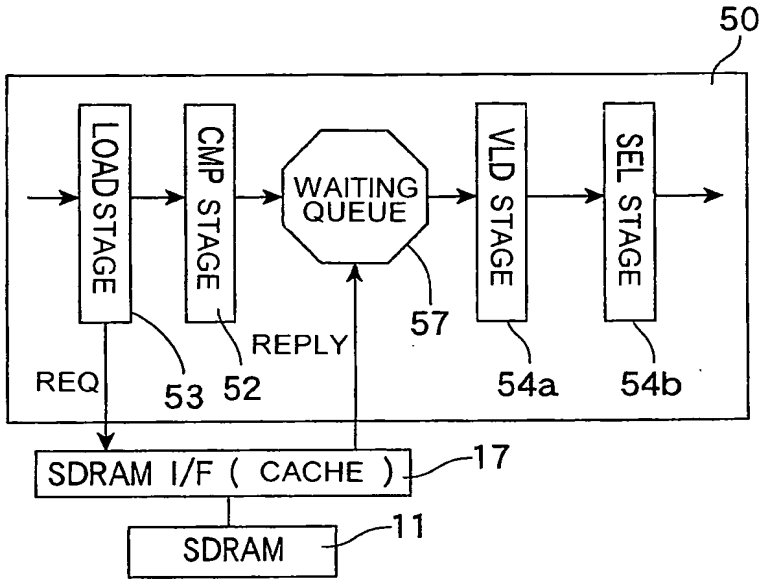

50
LOAD STAGE
CMP STAGE
WAITING QUEUE
VLD STAGE
SEL STAGE
REQ
53
52
REPLY
57
54a
54b
SDRAM I/F (CACHE)
17
SDRAM
11

FIG.67

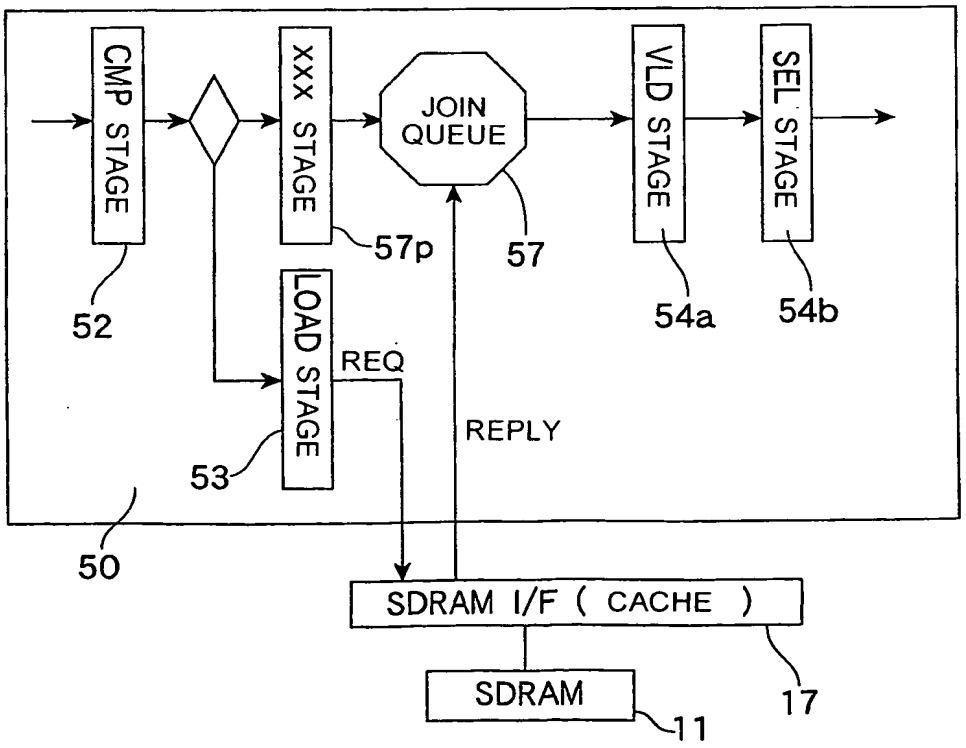

CMP STAGE
XXX STAGE
JOIN QUEUE
VLD STAGE
SEL STAGE
57p
57
52
54a
54b
LOAD STAGE
REQ
REPLY
53
50
SDRAM I/F (CACHE)
SDRAM
17
11

FIG.68

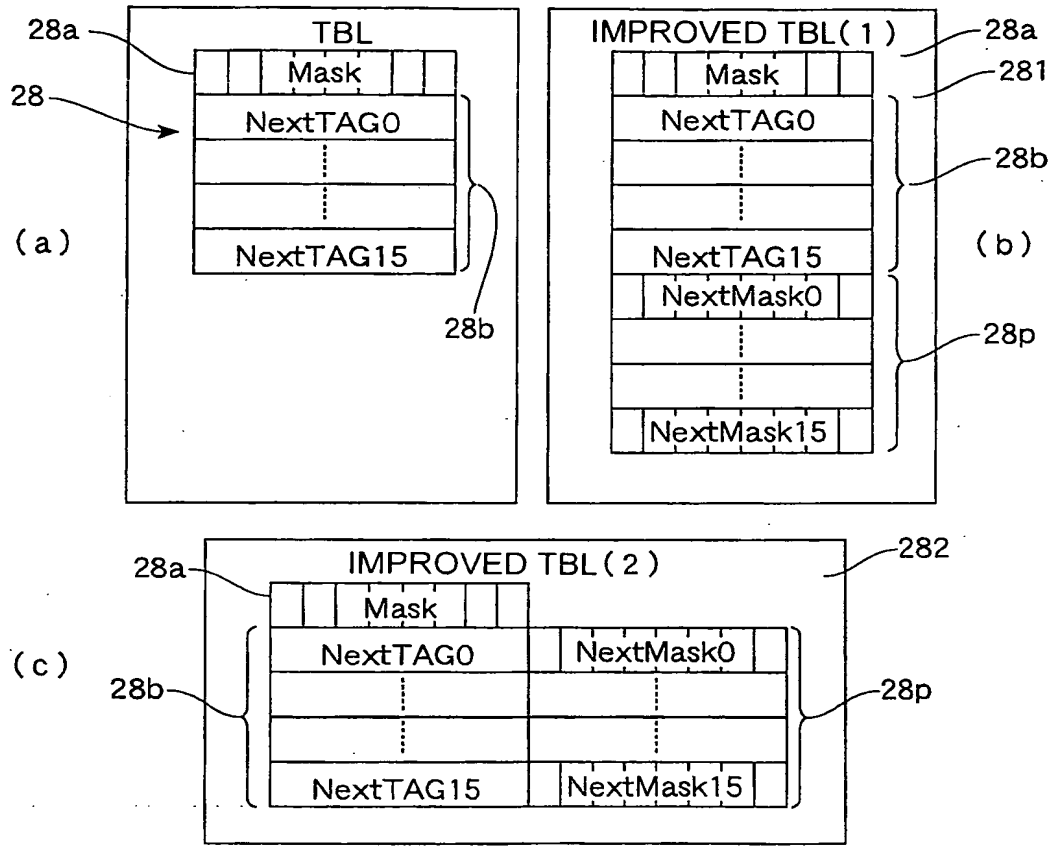

28a
TBL
Mask
28
NextTAG0
NextTAG15
28b
(a)
IMPROVED TBL(1)
28a
Mask
281
NextTAG0
28b
NextTAG15
NextMask0
28p
NextMask15
(b)
28a
IMPROVED TBL(2)
282
Mask
(c)
NextTAG0
NextMask0
28b
28p
NextTAG15
NextMask15

FIG.69

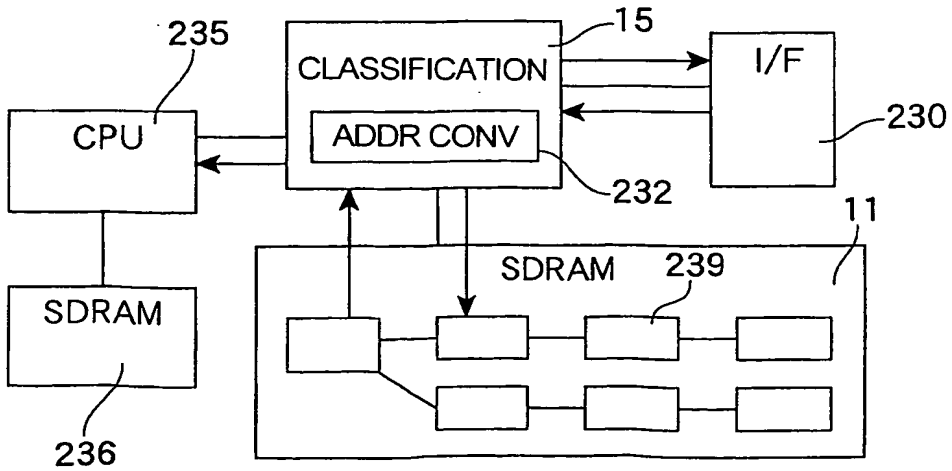

235
15
CLASSIFICATION
I/F
CPU
ADDR CONV
230
232
11
SDRAM
239
SDRAM
236

FIG.70

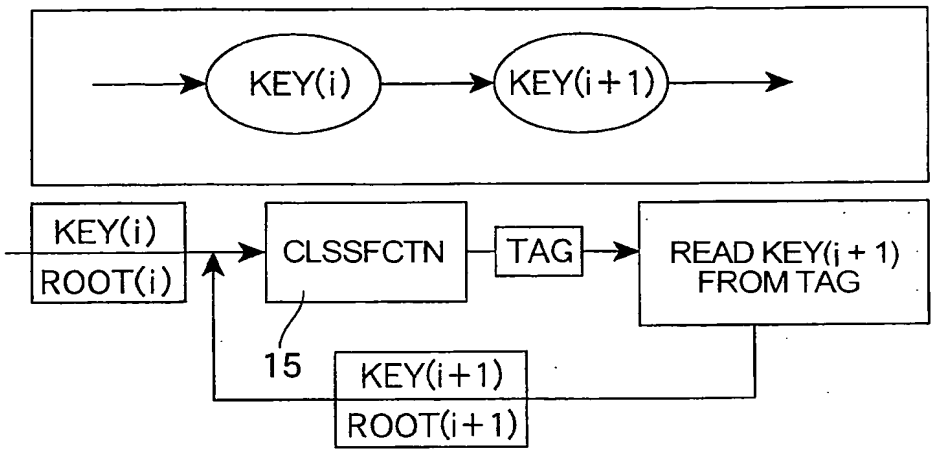

KEY(i)
KEY(i+1)
KEY(i)
ROOT(i)
CLSSFCTN
TAG
READ KEY(i+1) FROM TAG
15
KEY(i+1)
ROOT(i+1)

FIG.71

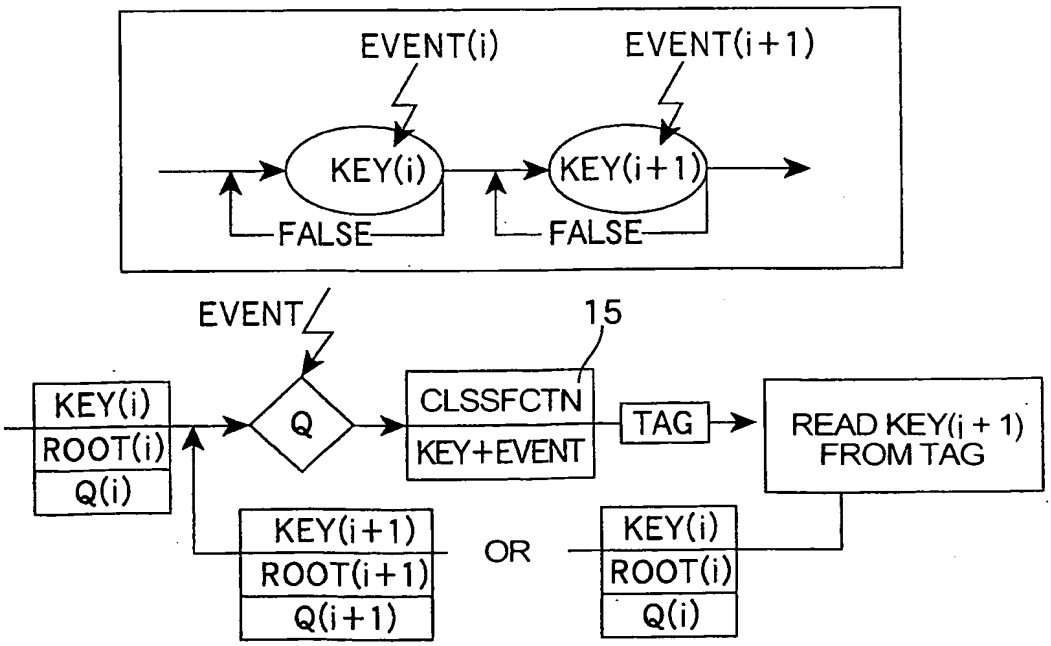

EVENT(i)
EVENT(i+1)
KEY(i)
KEY(i+1)
FALSE
FALSE
EVENT
15
KEY(i)
ROOT(i)
Q(i)
Q
CLSSFCTN
KEY+EVENT
TAG
READ KEY(i+1) FROM TAG
KEY(i+1)
ROOT(i+1)
Q(i+1)
OR
KEY(i)
ROOT(i)
Q(i)

FIG.72

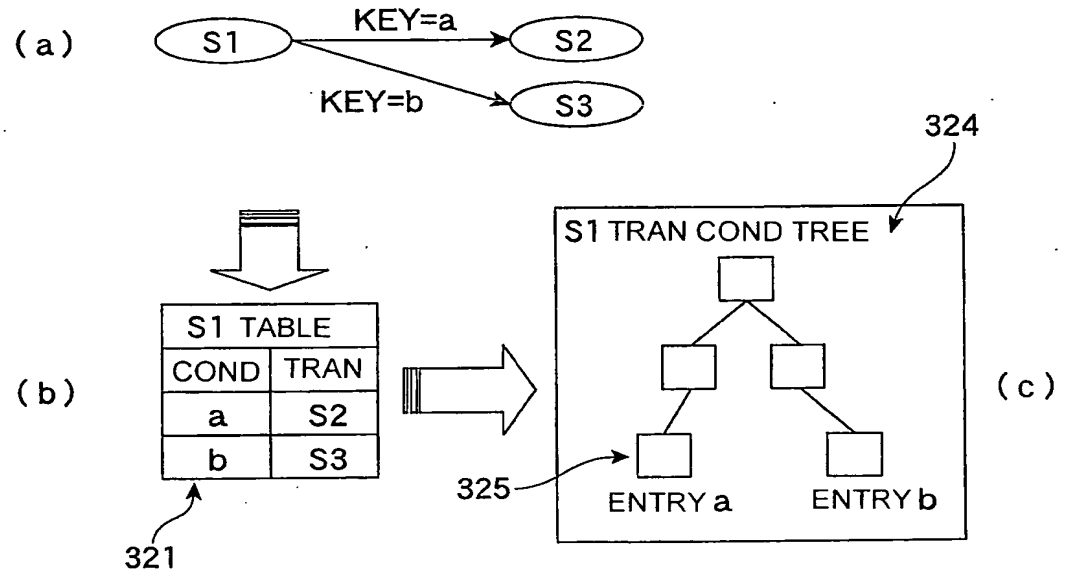

(a)
S1
KEY=a
S2
KEY=b
S3
(b)
S1 TABLE
COND
TRAN
a
S2
b
S3
321
324
S1 TRAN COND TREE
325
ENTRY a
ENTRY b
(c)

FIG.73

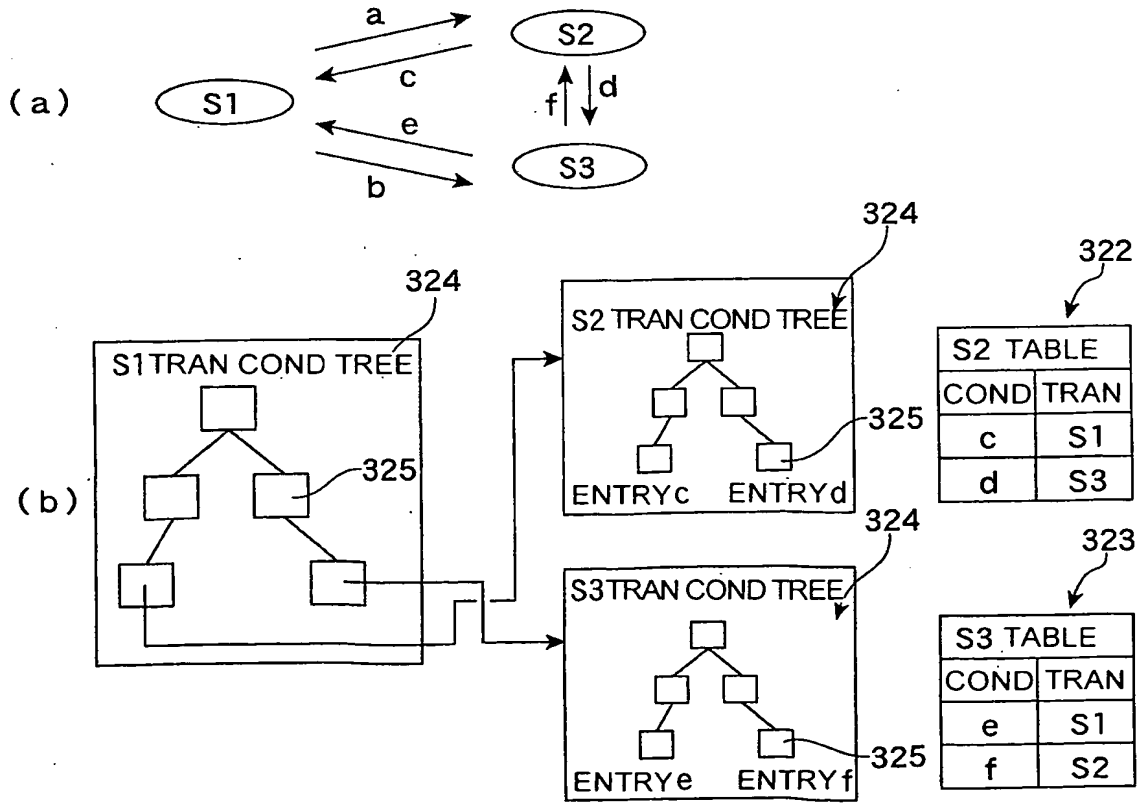

(a)
S1
a
c
e
b
S2
S3
f
d
(b)
S1TRAN COND TREE
324
325
S2 TRAN COND TREE
ENTRYc
ENTRYd
S3TRAN COND TREE
ENTRYe
ENTRYf
322
S2 TABLE
COND
TRAN
c
S1
d
S3
323
S3 TABLE
e
S1
f
S2

FIG.74

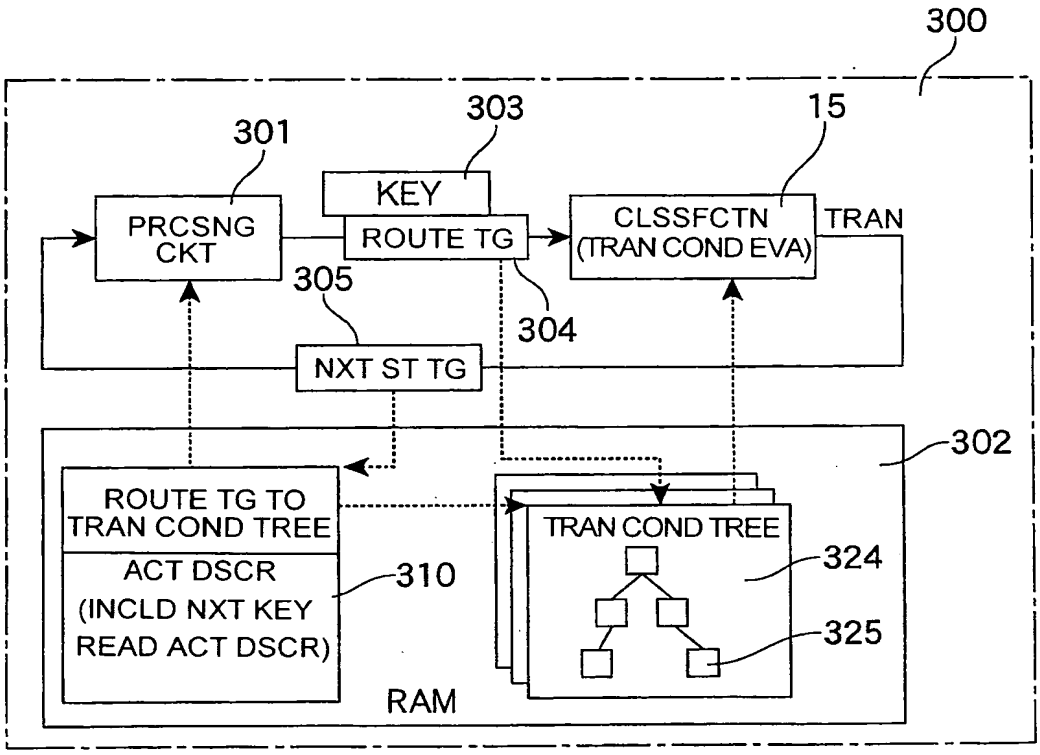
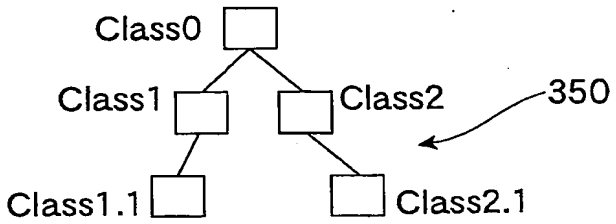

300
301
303
15
KEY
PRCSNG CKT
ROUTE TG
CLSSFCTN (TRAN COND EVA)
TRAN
305
304
NXT ST TG
302
ROUTE TG TO TRAN COND TREE
ACT DSCR (INCLD NXT KEY READ ACT DSCR)
310
TRAN COND TREE
324
325
RAM

FIG.75

(a)


Class0
Class1
Class2
350
Class1.1
Class2.1

(b)

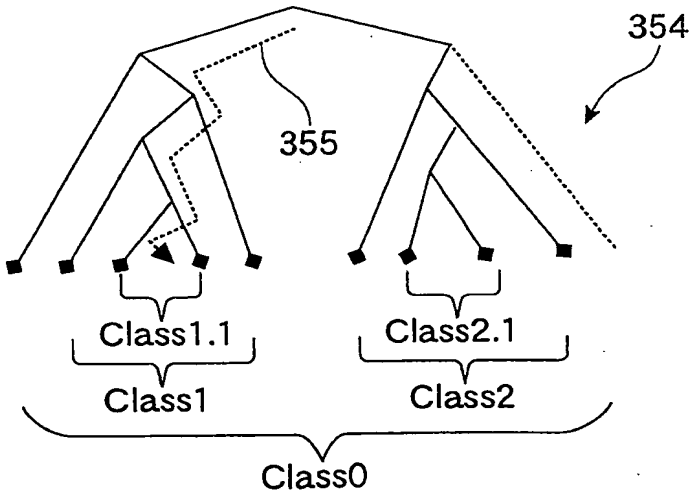

354
355
Class1.1
Class2.1
Class1
Class2
Class0

FIG.76

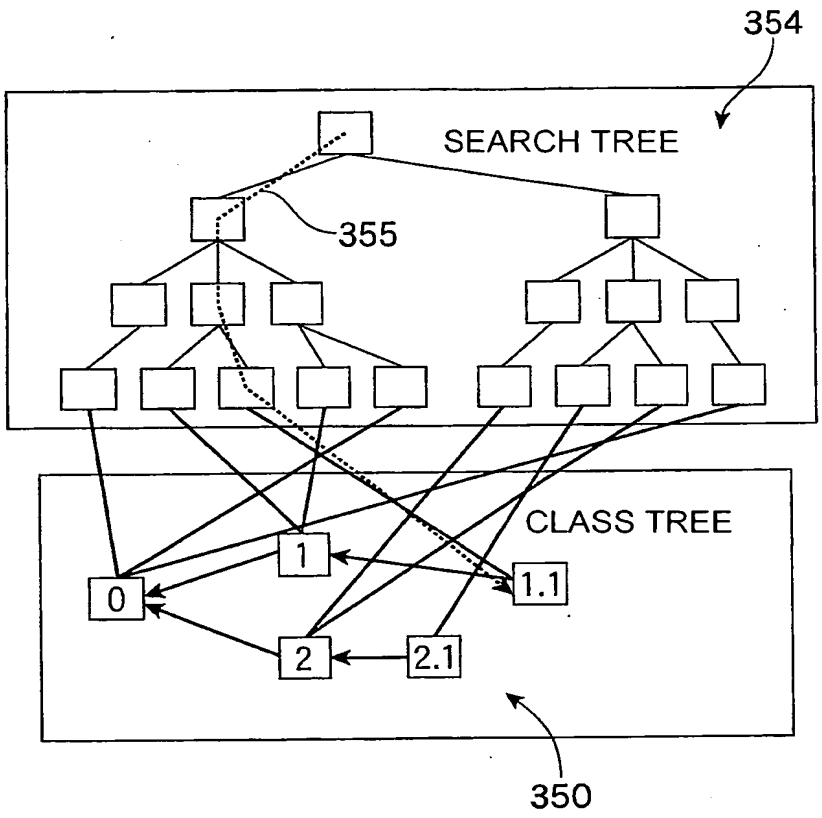


FIG.77

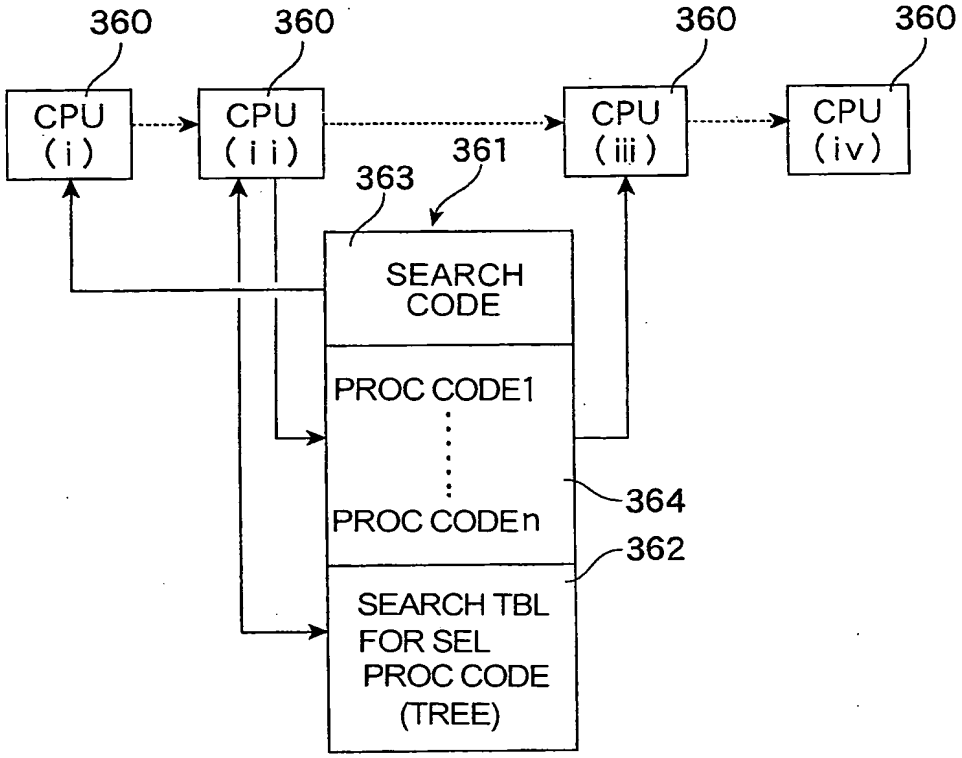
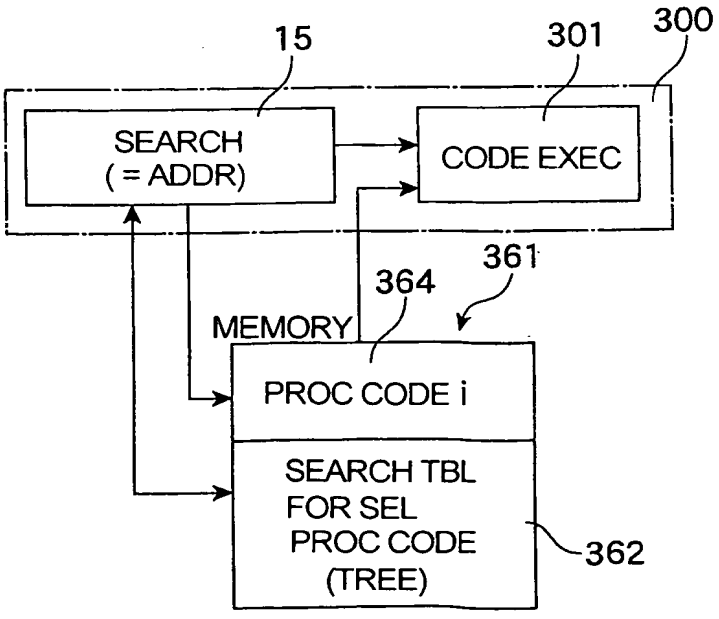

360
360
360
360
CPU (i)
CPU (ii)
CPU (iii)
CPU (iv)
361
363
SEARCH CODE
PROC CODE1
PROC CODEn
364
362
SEARCH TBL FOR SEL PROC CODE (TREE)

FIG.78


15
301
300
SEARCH (= ADDR)
CODE EXEC
361
364
MEMORY
PROC CODE i
SEARCH TBL FOR SEL PROC CODE (TREE)
362